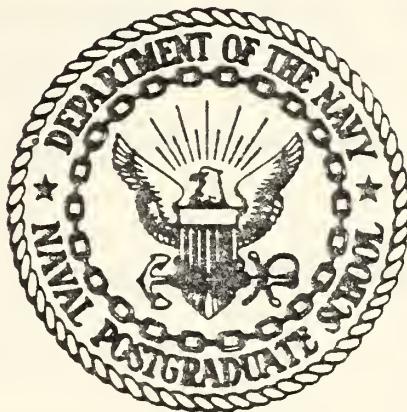


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THESIS

AN INTERACTIVE COMPUTER INTERFACE
WITH A DIGITAL RECEIVER

by

William Glenn Borries

March 1977

Thesis Advisor:

S. Jauregui

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An Interactive Computer Interface with
a Digital Receiver

by

William Glenn Bonries
Lieutenant, United States Navy
B.S., United States Naval Academy, 1970

Submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL
March, 1977

ABSTRACT

A computer interface to connect both the Applied Technology Airborne Computer (ATAC) and the KIM-1 Microprocessor to a Watkins Johnson digitally tuned receiver was designed and constructed. The existing ATAC computer program was modified.

TABLE OF CONTENTS

I.	INTRODUCTION -----	10
II.	THE RECEIVER -----	15
III.	THE COMPUTERS -----	22
	A. THE ATAC -----	23
	B. THE KIM-1 -----	25
IV.	THE INTERFACE -----	27
	A. CONTROL SECTION -----	29
	B. INPUT/OUTPUT REGISTERS -----	38
V.	THE PROGRAM -----	42
	A. MAIN SYSTEM -----	42
	B. RECEIVER CONTROL -----	45
VI.	RECOMMENDATIONS -----	50
VII.	CONCLUSION -----	51
	APPENDIX A: INTERFACE WIRING -----	52
	APPENDIX B: ATAC OPERATING INSTRUCTIONS -----	60
	APPENDIX C: ATAC PROGRAM ASSEMBLY -----	62
	APPENDIX D: SAMPLE ATAC OUTPUT -----	65
	APPENDIX E: CONVERSION PROGRAMS FOR THE ASSEMBLER -----	68
	APPENDIX F: ATAC PROGRAM -----	72
	BIBLIOGRAPHY -----	124
	INITIAL DISTRIBUTION LIST -----	125

LIST OF TABLES

I.	Problems and Solutions -----	14
II.	Receiver Modes and Periods -----	19
III.	Interface Command List -----	32
IV.	ATAC Program Commands -----	44

LIST OF FIGURES

1.	Computer Control -----	13
2.	The Receiver's Word -----	16
3.	Block Diagram of the Digital Section -----	18
4.	AIAC I/O Timing Diagram -----	24
5.	Interface Control Section (Part 1) -----	30
6.	Interface Control Section (Part 2) -----	31
7.	Interface Timing Diagram -----	35
8.	Input Register -----	40
9.	Output Register -----	41
10.	AIAC Program Block Diagram -----	43

LIST OF ABBREVIATIONS

A/D	Analog to Digital
ASCII	American Standard Code for Information Interchange
Baud	Bits per second
D/A	Digital to Analog
high	TTL logic 1 (+5v)
I/O	Input and/or Output
IC	Integrated Circuit
IF	Intermediate Frequency
ISR	Intermediate Sideband
low	TTL logic 0 (0v)
LSB	Lower Sideband
TTL	Transistor Transistor Logic
USB	Upper Sideband
RFO	Beat Frequency Oscillator

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I. INTRODUCTION

For many decades man has dreamed of the day when machines could relieve him of much of his work. In this era of computers and advanced technology, this dream is now becoming a reality. Connecting computers to other machines, however, is not just a simple matter of running a wire from one to the other. In order for the computer to be able to use its "thinking" ability, it must have some way to translate its signals into a form that is recognized by the machine it is controlling. This is where the interface becomes all important.

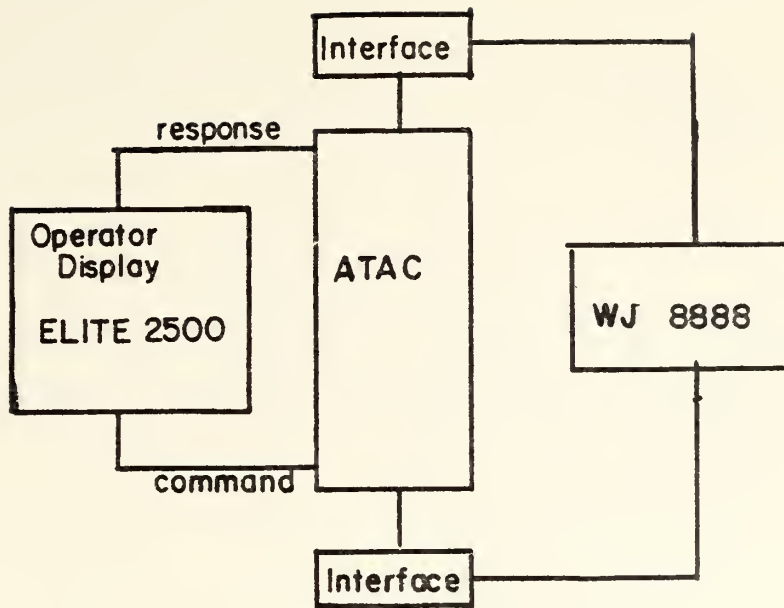
An interface is a piece of equipment placed in the data path between two devices. Its purpose is to rearrange, translate, or change the speed of this data to meet the needs of one or both devices. In other cases the interface is used to convert data from an analog to digital (A/D) or digital to analog (D/A) form, or both. Interfaces of either type range in complexity from a few integrated circuits to the use of microprocessors. Most, however, fall in between. This thesis discusses the design and construction of an interface in this middle class. Here, the computers are the Applied Technology Airborne Computer (ATAC) minicomputer and the MOS Technology Inc.'s 6801 microprocessor. Their goal is to program and process outputs from a digitally tunable Watkins Johnson WJ-8888.

The two computer systems arrive at their goal by

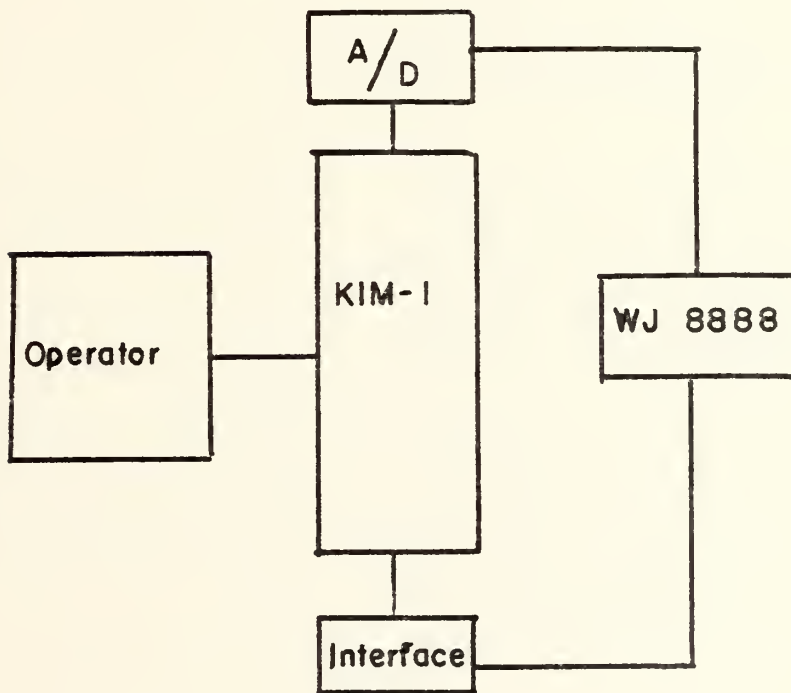
different means. The ATAC uses a closed loop with the operator (Figure 1a) while the KIM-1 excludes the operator while executing its program (Figure 1b). In the ATAC loop the operator actively controls all communication between the computer and receiver. In this way it is possible to display information from the receiver on the video display at any time except during a scan (see Chapter V). It also provides quick reference to the data to be sent, the data last sent, and latest received data. This was invaluable during debugging. From the terminal it is also possible to adjust available parameters as necessary to meet any requirement.

The KIM-1 does not directly exchange digital words with the receiver, but rather exchanges digital data for analog data. This does not provide a feedback loop that includes the operator. Once begun, the KIM-1 program selects and sends data words to the receiver and processes the analog data received until the program comes to an end or is halted by the operator. Direct information is not available to determine when or if a digital word has been sent or received correctly.

Problems encountered during the design and construction of the interface and their solutions are shown in Table I. In this instance signal level compatibility was not a problem because the I/O from the receiver, the interface, and the two computers were all TTL logic levels and, therefore, matched. It is believed that these problems are a typical list that may be encountered when interfacing.



(a)



(b)

Figure 1
Computer Control

PROBLEM

SOLUTION

1. Noise on the ATAC I/O lines.

1. Use of Schottky circuits reduced or eliminated the noise.

2. Different clock rates of the computers and the receiver, and different data word lengths.

2. ATAC; converted parallel outputs into serial form. KIM-1; used interrupt lines to slave the KIM-1 to the receiver's clock.

3. Timing

3. Identified receiver periods by the Monitor Clock output. This provided a pulse which signaled stable data.

4. Inputting data to the ATAC.

4. Open collector buffers were used to sink the required current for proper data transfer.

5. Switching between the ATAC and the KIM-1.

5. Multiplexers and buffers were used to switch between the two computers.

Table I

Problems and Solutions

II. THE RECEIVER

The Watkins Johnson WJ-8888 (WJ) is an HF receiver designed for use in the 550 KHz to 30 MHz band. Its advantages include the ability to detect and output both the AM and FM IF signals while simultaneously maintaining a separate output of eight selectable detection modes. Options available to the operator include different IF bandwidths, variable RF gain, squelch control, and a tuneable BFO frequency. The WJ is digitally controlled and uses a 64-bit word as shown in Figure 2. This word contains the information necessary to transfer the frequency, detection mode, IF bandwidth, RF gain, BFO frequency, and signal strength both internally and externally.

All inputs and outputs from the receiver are controlled by the synchronous, remote I/O board. This board is a gated transfer point for all digital data exchanged with the receiver. A number of control lines are needed to provide the necessary demands on the receiver. Three balanced input pairs and four balanced output line pairs, plus a ground are provided for this purpose. All three inputs are required for remote operation. They are address (or enable), trigger, and data input. The address pair is the most important for it serves as the master "on-off" switch for the remainder of the I/O pairs. The outputs furnish the required clocks (command and monitor), output data, and a local/remote status.

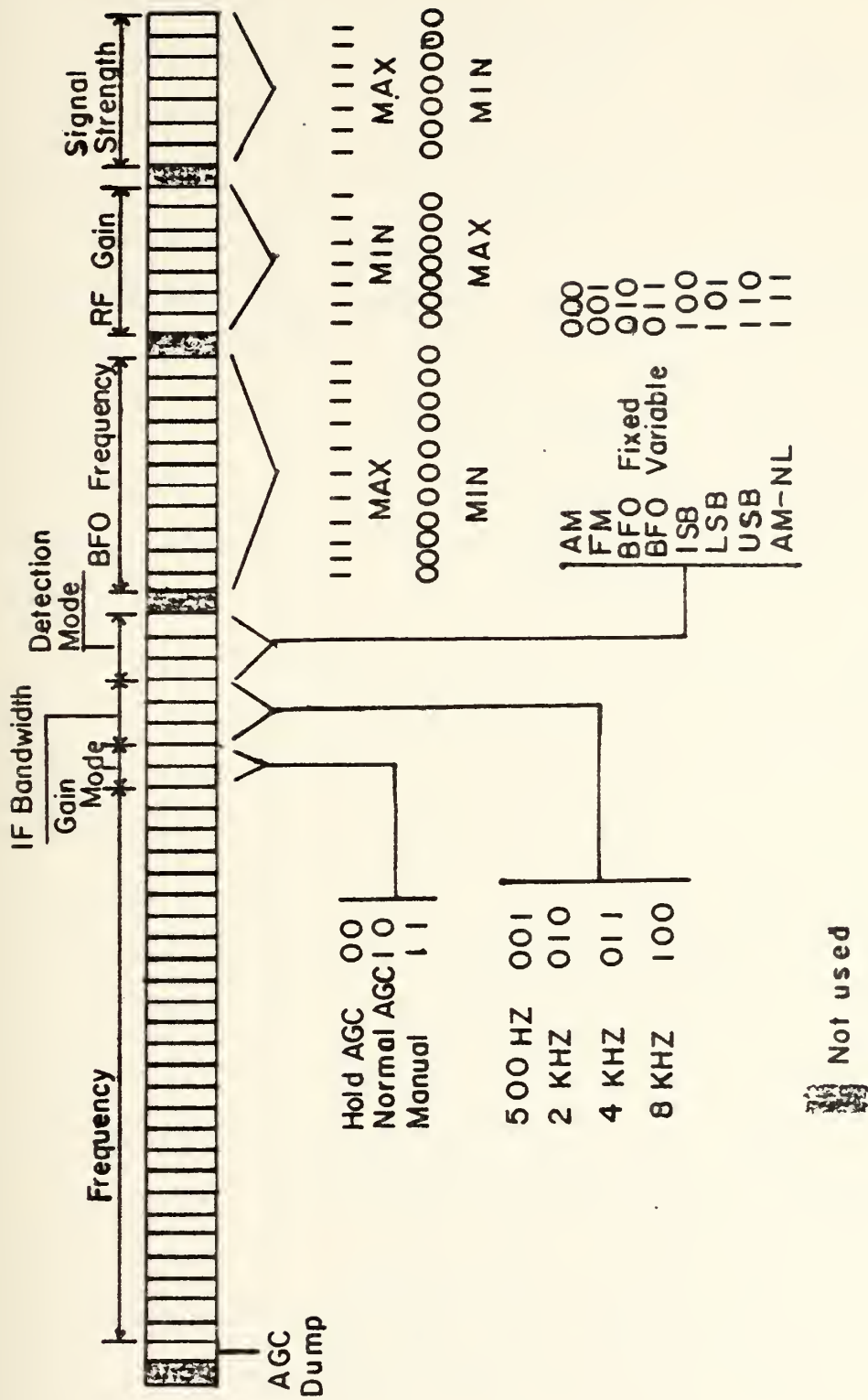


Figure 2
Receiver's Word

The Watkins Johnson operates on a sequential cycle divided into four equal periods and six identifiable modes. The periods regulate the different operations while the modes ascertain the origin of the data. Table II shows the interaction of the periods and modes of the receiver. Three of the six modes are memory read and write functions; these cannot be remotely controlled and, therefore, are of no concern here. Of the remaining three, two are the remote active and remote passive modes. These allow the introduction of externally generated data and prevent manual intervention during all but one of the four periods. Manual control is available in the remaining mode, local.

In order to manage the data word movement correctly, the receiver utilizes a common bus or data node arrangement as shown in Figure 3. This simplifies operation by forcing all data words to pass through this node in the same direction, regardless of their origin or desired destination. The multiplexer controls the input to the data node. Control of the multiplexer and, therefore, the origin of the data is managed by the internal modes of the receiver. The objective of period one is to load the receiver register. In the local and remote passive modes, the data word is shifted from the front panel register, through the multiplexer and data node, into the receiver register. The difference between these two modes is in the action of the data prior to shifting. The local mode updates the data word from the front panel storage registers during the early

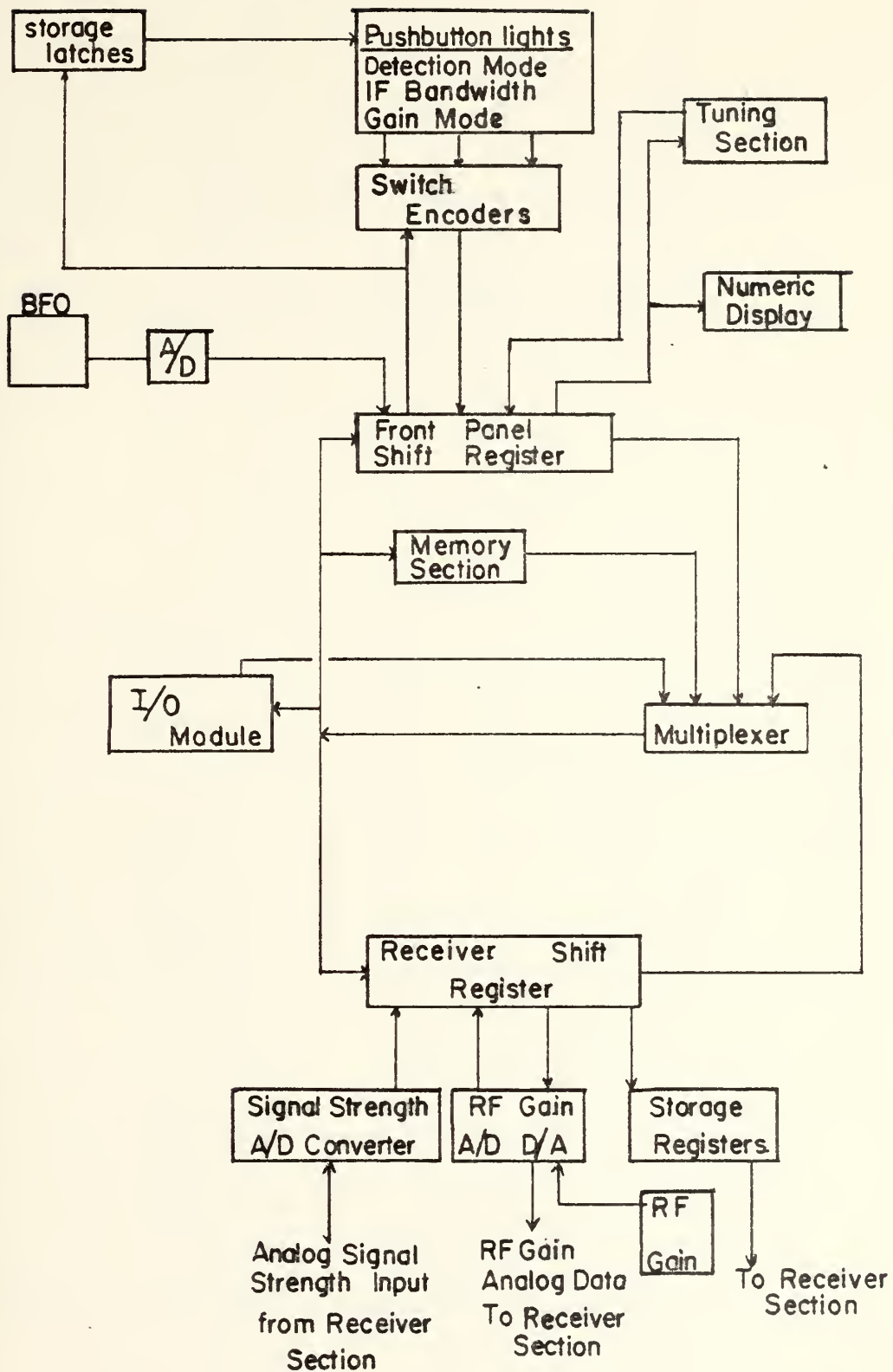


Figure 3
Block Diagram of the Digital Section

Local	Period			
	1	2	3	4
Remote Passive	Load Front Panel Reg from Front Panel/word shifted to Receiver Register	Load Rcvr Storage Key/ Signl Strength and RF gain updated /word shifted to FrontPanel Register	Display updated no words shifted	Change to Remote Active or Remote Passive possible
	Word shifted from FrontPanel Register to Receiver	Update only Sig Str /Load Rcvr Storage Reg/word shifted to FrontPanel Reg.	Same as Local	Change to Lcl or Remote Active possible
Remote Active	Word shifted from I/O module to Receiver Register	Same as Remote Passive	Same as Local	Change to Remote Passive automatic. Change to Local possible

Table II

Receiver Modes and Periods

portion of period one. This action is inhibited during the remote passive mode. In the remote active mode the data word originates from a remote device, is shifted by the command clock through the remote I/O board, on to the receiver register via the multiplexer and data node.

The first part of the second period is spent loading the data shifted during period one into the receiver storage registers. During this time the signal strength is updated in the receiver register regardless of the mode. The RF gain A/D-D/A converter functions according to the selected mode. In the local mode the RF gain bits in the data word are replaced by A/D conversion of the front panel RF gain control knob. The two remote modes reverse this action and load the RF gain D/A converter with this data from the word. After this is completed, the word is shifted in all modes out of the receiver register, through the multiplexer and data node, and into the front panel register. If the address line from the remote device is active high, the data word and the monitor clock are available on their respective output line pairs.

Periods three and four inhibit movement of the data word. Period three updates the front panel pushbutton lights and numeric display. Period four is the only period in which changes in receiver mode are allowed. During this period changes from a remote mode to local, or from local directly to remote passive can only be accomplished by depressing the appropriate pushbutton on the front panel. A

change from local and remote passive to remote active is automatically done by the remote I/O board whenever both the address and trigger line pairs are active high during this period. The remote active mode immediately reverts to the remote passive mode at the beginning of the next period four. The total cycle time of the receiver is 10.24 msec (2.56 msec per period). In order to change modes successfully, it may be necessary either to hold in the pushbutton or to hold the trigger and address lines high for up to 7.68 msec (three periods). This ensures that the mode change demand occurs in period four.

All outputs are available from connectors J1, and J6 through J10 located on the back of the receiver. J1 is the digital I/O connector. The other connectors are all analog outputs. J6 is a 455 KHz IF signal of at least 20 KHz bandwidth. AM and FM detector monitors are provided at connectors J7 and J9 respectively. J8 is a predetection, 455 KHz center frequency IF output whose bandwidth is set by the front panel. A balanced and unbalanced line audio and both upper and lower sideband outputs are available from the appropriate pins at J10. The balanced line operates at all times. The unbalanced line is operable unless headphones are plugged into the front panel. The lower sideband output is active when the receiver is in either ISB or LSB detection modes, and the upper sideband output is active during ISB, USB, and CW modes.

III. THE COMPUTERS

After studying the inputs and outputs from the receiver, three choices were available for further development of the interface. It could be designed to pass the clock pulses on to the interrupt lines of the computer and, therefore, match the computer's timing to that of the receiver. Or, a buffer could be constructed to input the data serially at the clock rate of the computer and output it at the clock rate of the receiver. The third choice, also a buffering arrangement, could exchange data in parallel to the computer and serially to the receiver.

The chief factor influencing the design decision was the availability and distribution of computer control and I/O lines. For the first computer, the primary objective was to investigate the feasibility of both remotely tuning the receiver and accepting a data word in return. The requirements for the second computer, the MOS Technology Inc. KIM-1, were less strict. Its objective was to tune the receiver digitally through use of the interface. Its input, however, was to come from a A/D converter for processing.

A. THE ATAC

The ATAC was originally designed to provide EW service to aircraft. Built to do real-time analysis of signals, it has very short cycle times, optional microcode programming, and double precision arithmetic as part of the standard package. All this, combined with its large instruction set, makes the ATAC a versatile and powerful tool. Although data could be transferred serially by proper programming, the ability of the ATAC to both input and output sixteen bits in parallel on the PIO (parallel input/output) lines proved more advantageous. Any one of the ATAC's sixteen registers can input or output from these lines. In order to properly transfer this data, the PIO bus must be augmented by an address provided by the sixteen bits of the "extended" Arithmetic Register (XAR). Another necessary output is one that informs the external device when the ATAC is ready for the transfer. On the ATAC this function is provided by the Input/Output Demand (IOD) line. Referring to the timing diagram in Figure 4, an input command is initiated by placing an address on the XAR lines and following this address with a low on the IOD. This signifies that the ATAC register is ready for data. After approximately one microsecond, the IOD is placed high and the address is removed. During this microsecond the data for the ATAC must be stable. For an output command, the XAR and the PIO lines first present the address and data for output. When they

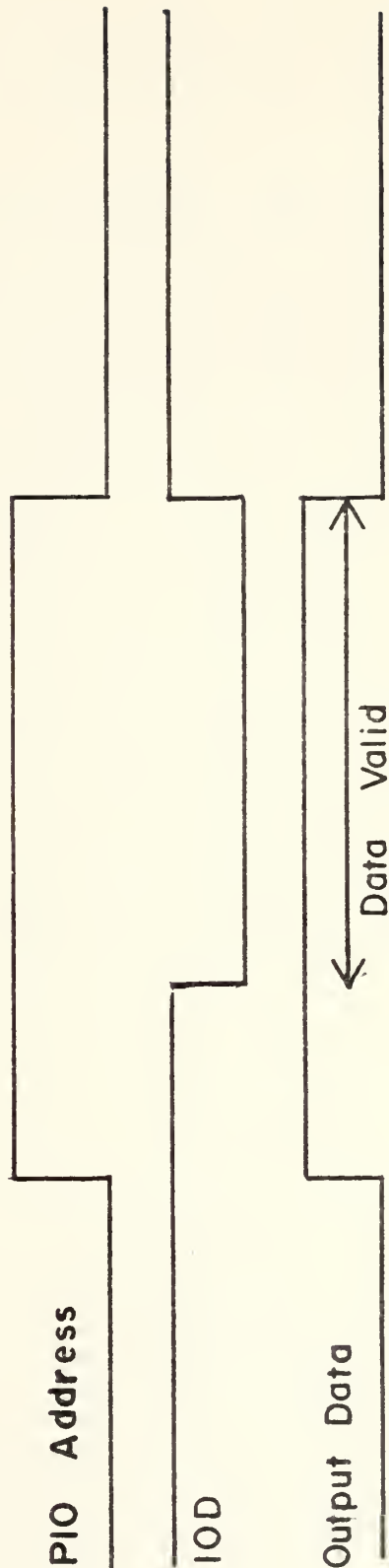
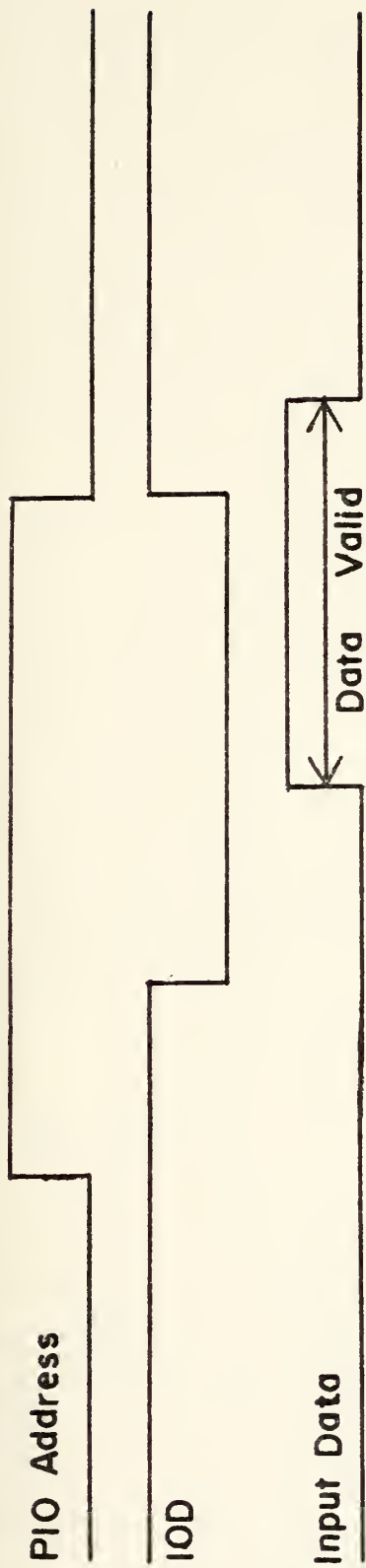


Figure 4
ATAC I/O Timing Diagram

are stable, the IOD line is set low. The data is then available for about a microsecond, as before. The IOD line is then placed high and the address and data are removed from their respective lines.

For operator interaction a serial ASCII, RS232 I/O port is also available. A Datamedia Elite 2500 television terminal is connected here to provide the operator with the necessary control and programming capability for use of the ATAC. By proper programming and use of the XAR lines, it was possible to translate each command for the interface. Using a demultiplexer on the interface board, four of the five available XAR addresses were separated into sixteen separate commands. One of the remaining lines and the IOD line were used as strobes to identify the receiver and to signify stable data (Chapter III). This arrangement provided both the adequate isolation and flexible operation desired.

B. THE KIM-1

The KIM-1 is at the other end of the computer spectrum with respect to the ATAC. It is a microprocessor designed around the MOS Technology Inc. series MCS8500 Central Processor Unit. Complete on a single printed circuit board, the KIM-1 is simple to operate and easy to program. While its cycle time is slower than that of the ATAC, it is still much faster than the receiver and more than adequate to meet

the requirements. Since the input data came from converted analog data supplied from the receiver's FM IF output (J9) and an external A/D converter, the design for this portion of the interface was simpler.¹

¹For a more detailed discussion of the KIM-1, its objectives, programs, and operating procedures, see Signal Acquisition and Sampling Using a Microprocessor, by LT. D. Rosenbender.

IV. THE INTERFACE

The interface was initially designed solely for the ATAC. A means of converting four ATAC words into one receiver word was needed first, in order to test the program, the computer, and the receiver together. The simplest and cheapest way to accomplish this conversion and still fully utilize the capabilities of the ATAC was to build a 64-bit register using eight parallel-in, serial-out, eight-bit shift registers. A control section was also necessary to properly handle this data. The ATAC XAR addresses were decoded by this control section to provide the load commands for the registers and to signal the receiver to input the word.

The next step in construction was also simple in theory. Since the computer uses the PIO lines for input as well as output, what was needed was a connection which would not interfere with the section already built. The ICs chosen to isolate the two sections are called Tri-State. These ICs have a "no output" state in addition to the normal high and low of TTL circuits. They could not, however, sink or supply enough current to drive the computer PIO bus. A solution was found by following these ICs with open collector buffers. Not only did they provide the necessary amplification, they did not degrade the isolation performance of the Tri-States. This second section also had

a 64-bit register built from the smaller shift registers. In this case, though, they were serial-in, parallel-out. In order to remove the word from the register in sixteen-bit sections, the outputs from the shift registers were connected to four-to-one multiplexers. These multiplexers were Tri-State. With the proper control it was possible to shift the word from the receiver into this register, and transfer it to the PIO bus in the correct sequence.

Increased complexity in the control section came with this implementation. A method was needed to prevent the computer from transferring a word until it had been completely shifted into the register. The period two clock output from the receiver was used as a reference to provide a pulse to inform the computer when shifting was complete. This pulse was positioned in the same time interval as period three of the receiver. The additional benefit of identifying period four was obtained. This meant that the output for the tridden line to the receiver could be shorter and still meet the requirement to occur in a portion of period four.

After completion of the testing for the ATAC, an interface was designed and constructed for the KIM-1. This design was very simple to implement, since all the necessary timing circuits were already built and tested. The two computers were kept from interfering with each other by installation of a manual switch. This switch controls the

address of a multiplexer that separates the lines in the interface common to both computers. The control section was wire-wrapped rather than placed on a printed circuit board to provide greater flexibility, easier maintenance, and to reduce cost.

A. THE CONTROL SECTION

The heart of the interface is the control section (Figures 5 and 6). The main purpose of this section is to decode and route commands from the ATAC and provide the necessary circuits to interface with the receiver. It also contains the circuits for the operation of the receiver by the KIM-1. The receiver's outputs are driven by line drivers which provide complementary TTL levels. The inputs are applied to line receivers which accept these complementary TTL levels. The interface, therefore, had to use these same receivers and drivers to be compatible with the Watkins Johnson.

The SPST switch mounted on the front of the interface case selects the computer controlling the receiver. With the switch in the ATAC position, a high is placed on pin 1 of IC-JJ and pins 1 and 10 of IC-MM. IC-JJ is now set up to transfer the following: the address and data outputs to the line drivers on IC-LL, the trigger command to pin 2 of IC-Z, and a low in line CCK7. The CCK7 line completes the

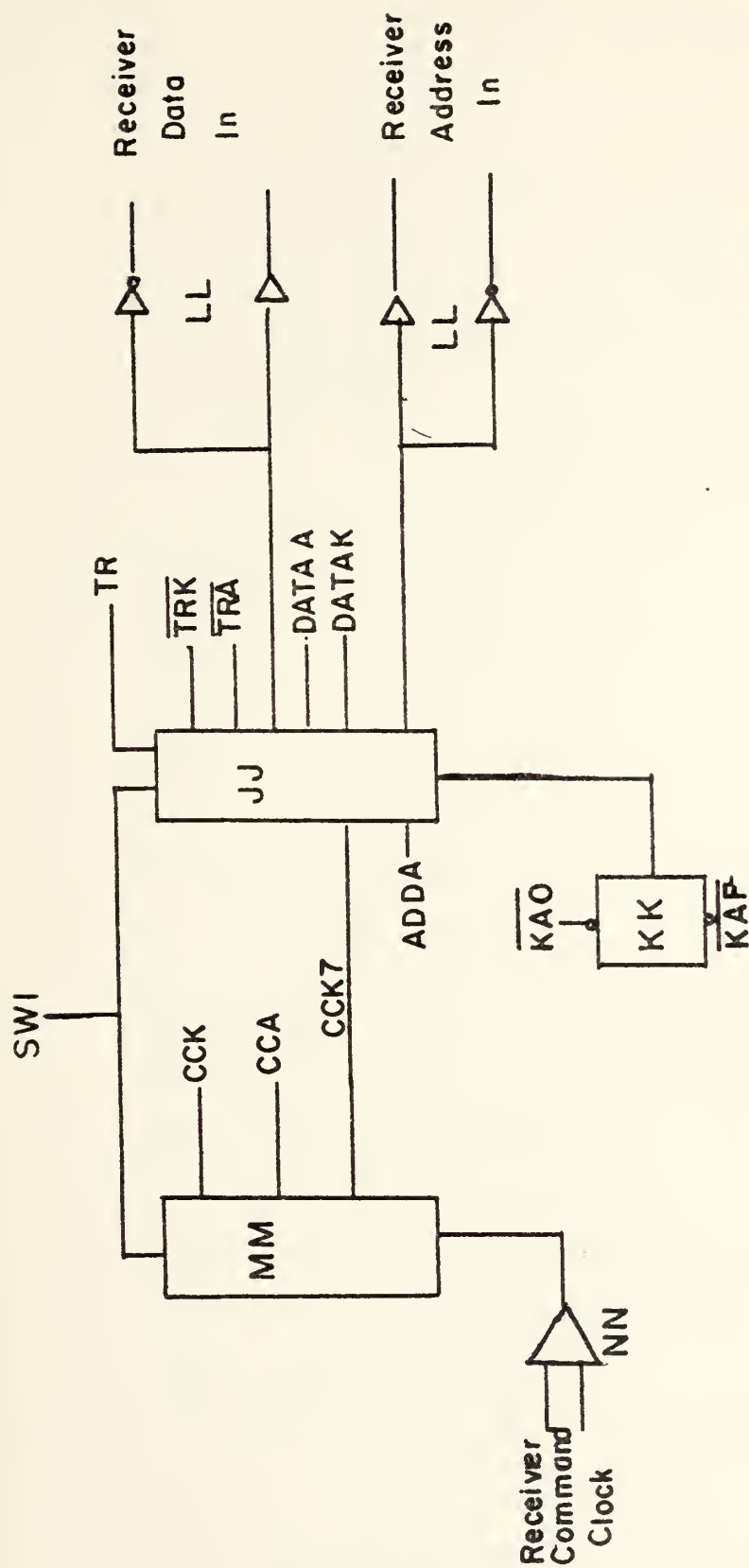


Figure 6
Interface Control Section (Part 2)

TRA	[0]	ATAC Trigger Command
DIA	[1]	Receiver input word one
DIB	[2]	Receiver input word two
DIC	[3]	Receiver input word three
DID	[4]	Receiver input word four
DSP	[5]	Stop Monitor Clock
DST	[6]	Start Monitor Clock
ADD	[7]	ATAC - Address on
DOA	[8]	Receiver output word one
DOR	[9]	Receiver output word two
DOR	[9]	Receiver output word two
DOC	[10]	Receiver output word three
DOD	[11]	Receiver output word four
RDY	[12]	Read D11 for ready signal
ADF	[15]	ATAC - Address off
TR		Receiver trigger
CCK		KIM-1 Command Clock
CCK7		Control Line for KIM-1 Command Clock
CCA		Command Clock for ATAC interface
ADDA		ATAC - Receiver Address
KADD		KIM-1 - Receiver Address
KAO		KIM-1 - Receiver Address On
KAF		KIM-1 - Receiver Address Off
TRK		KIM-1 Trigger Command
(Numbers in brackets refer to ATAC XAR commands)		

Table III
Interface Command List

commands to IC-MM. This IC is a quad Tri-State buffer which is used to control the destination of the command clock. The switch opens buffer one which directs the command clock to the ATAC. The CCK7 line closes buffers two and four disabling the command clock input to the KIM-1.

The ATAC supplies the control section with six lines. Five of these are the XAR bits 4,5,8,9, and 13. Using 4, 5, 8, and 9 as address lines to pins 20-23 of IC-DD, a four-to-sixteen demultiplexer, sixteen (2^4) unique commands (Table III) were made available. The sixth line, the IOD, and XAR 13 were used as strobes or enables for the demultiplexer. In this way XAR 13 was able to specify this receiver uniquely, and the IOD ensured that addresses and data were stable before passing a command. When both IOD and XAR 13 are low, IC-DD is operational and the output corresponding to the address on pins 20-23 is forced low. At any time that either or both the two strobe lines are high, all outputs of IC-DD are held high and no commands are generated, regardless of the activity on pins 20-23.

At the beginning of the Receiver Control program (Chapter IV), the ATAC sends commands to address the receiver (ADD) and to open the gate for the monitor clock (DST). ADD places a low on pin 2 of IC-E, setting the flip-flop and forcing the ADDA line high. This line activates the receiver's I/O through ICs -JJ, -A, -B, -C, and -LL, as described above. The DST command is passed to

pin 7 of IC-E. This sets this flip-flop and allows the monitor clock (MC) to shift data from the receiver into the storage register during every period two of the receiver's cycle. The MC line is also connected directly to a timing circuit. This circuit produces the pulse described in the early part of this chapter. The first of a pair of monostable multivibrators, IC-Y (Figure 5) is triggered by the first clock pulse of MC. IC-Y outputs a pulse, interval A of timing diagram (Figure 7), which triggers the second. The second's output, interval B, is connected to pin 1 of IC-II, a negative-edge triggered, J-K flip-flop. This IC is wired so that it is set on the output of the second multivibrator and reset by either the the output of the first multivibrator or the command TR. The output of this flip-flop, pin 15, is called the RLP. This line is multiplexed with the least significant bit of the output register and inverted by IC-H for use by the ATAC on line D11.

The RLP pulse is adjustable through variable resistors (trimmers) one and two. Trimmer one controls interval B and trimmer two interval A. In effect, trimmer two varies the position of the pulse and trimmer one its width. The placement and width are the key to proper operation of the interface. The pulse must remain in period three. Although some overlap into period four is allowable it is not desirable, and any overlap into period two could cause

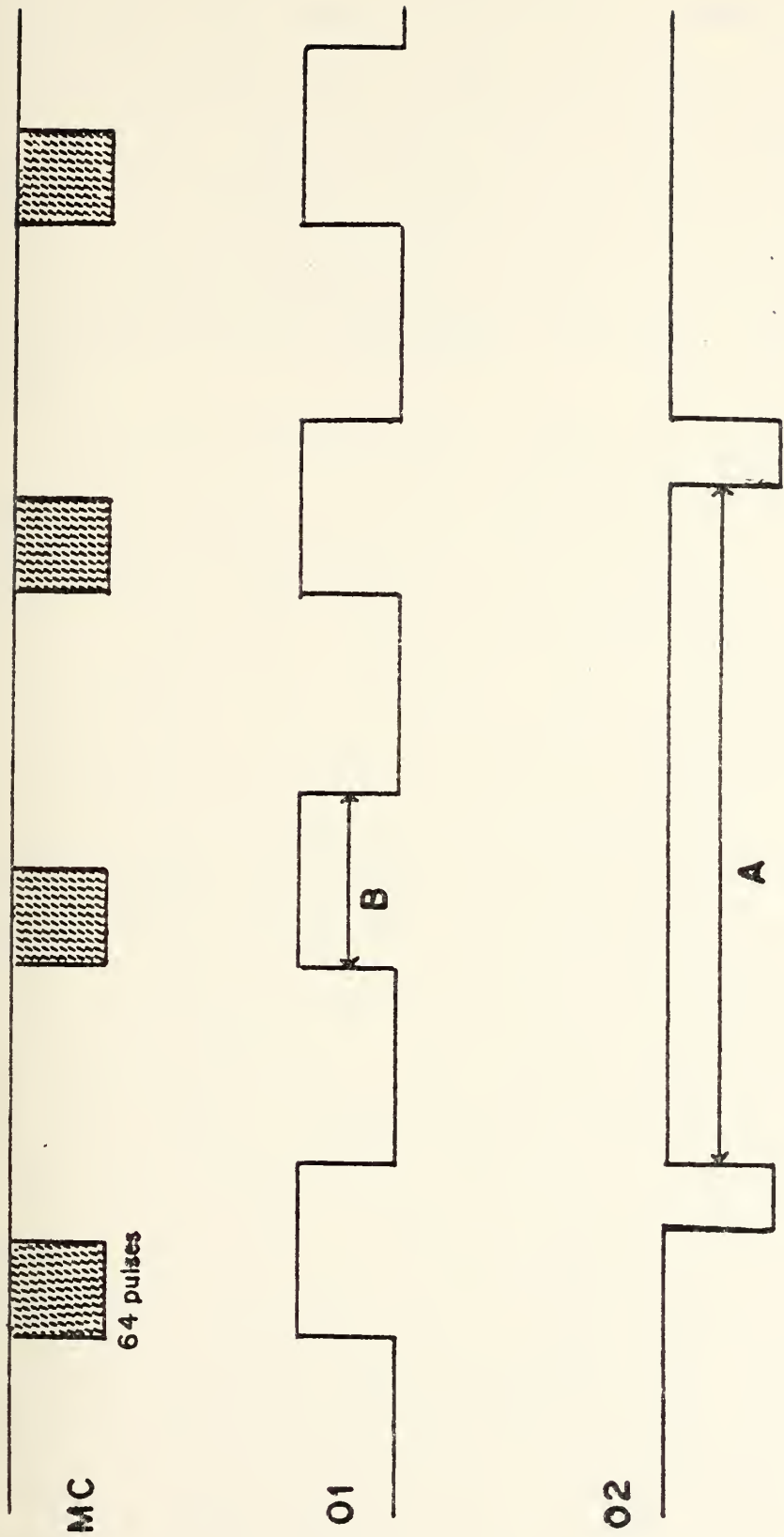


Figure 7
Interface Timing Diagram

incorrect operation. At present, the RLP pulse is programmed for every other period three. This allows the receiver to stabilize between samples taken by the computer. If more or less time is desired, the pulse can be set in every, every other, or every third period three by varying trimmer one. Greater time between pulses can be achieved by changing the .47 uF capacitor (6H-7,8) to one of larger value.

When the ATAC is ready to send a word, it loads the input register of the interface using commands DIA, DIB, DIC, DID, and then waits for a high on the D11 line. When RLP is low, D11 is high and the ATAC sends command IRA. This command is routed to a separate monostable multivibrator, IC-Z, by way of multiplexer IC-JJ. The timing circuit provides the trigger pulse in period four which changes the receiver's mode to remote active. It also sets RLP high to prevent any interaction with the ATAC until this cycle of the receiver is complete. During the following period one, the receiver sends the command clock to the input register via ICs -JJ and -MM, and inputs the data word through ICs -IJ and -LL. Meanwhile, the ATAC is waiting for RLP to go low again. When it does, the ATAC closes the MC gate with a DSP command and loads four sixteen-bit words with commands DDA, DDB, DDC, and DDD. Once the receiver word is stored in the ATAC, a DSIA command is sent to open the MC gate. When the operator has finished execution of the Receiver Control program and exits, the ATAC

sends the interface commands ADF and DSP to turn off the address line to the receiver and close the MC gate. The interface is now back in a stand-by status.

In order to set up the interface for operation with the KIM-1, the reset button must be pushed and the computer switch placed in the KIM-1 position. The reset button is unique to KIM-1 interface operation, and is necessary because of the use of the KIM-1's non-maskable interrupt. This interrupt is used to synchronize the KIM-1 with the receiver's command clock. Pressing the reset button places a momentary low on pin 5 of IC-rK, the flip-flop that controls the receiver's address line from the KIM-1. This resets the flip-flop and insures that the command clock output is disabled until required. ICs -JJ and -MM now transfer data from the KIM-1 and not the ATAC. The CCK7 line follows the address line from IC KK and gates the command clock off and on at the proper time. When the KIM-1 is ready to send a word to the receiver, it waits for a low on the RLP line. This line is connected to the maskable interrupt line. This low generates an interrupt and places the KIM-1 in the output program. This routine provides a trigger pulse for the trigger timing circuit and outputs the data synchronously with the command clock. The difference between the ATAC and KIM-1 actions of the interface is due to the position of the switch. The only function the interface serves is to provide reliable and compatible data to the appropriate device, whether it is receiver or

computer.

B. INPUT/OUTPUT REGISTERS

These two registers are used for the ATAC only. The registers were designated input or output by their related function with the receiver. They were constructed to provide the necessary, temporary storage while converting parallel and serial data back and forth. Both registers are connected to the PIO bus, with the major difference being the Tri-State connections of the serial to parallel, or output register.

The input register (Figure 8) was the easier to implement. It consists of eight 8-bit shift registers with parallel input and serial output. The parallel input comes from the ATAC's PIO bus, which is buffered by schottky inverters to reduce noise. The lines are connected to the ICs in such a way as to load words into two adjacent shift registers simultaneously. This is possible because the shift registers will only latch data in when their respective load line is low. By proper connection of the DIA-DID lines to pin 1 of the ICs, and coordinating the commands with the data, the output register can be completely and correctly filled. The command clock from the receiver is connected to pin 15 of each of the eight registers. When it is present, it clocks the data through the register exiting through pin 16 of IC-VV. From here, it goes through the control section

at IC-MM and on to the receiver.

The output register (Figure 9) performs the reverse operation. However, in order to separate it into words that are short enough for the ATAC, the data has to be multiplexed before it can be connected to the PIO bus. The Tri-State multiplexers, ICs -I through -L and -U through -X, and the required buffers, ICs -EE through -GG, were used to prevent interaction with the PIO bus when not in use. The timing here is more critical than in the input register system. Before the ATAC begins a read cycle from the output register, the clock signal to the register is stopped (DSP). This prevents the ATAC from reading non-stationary data. All the Tri-State multiplexers are addressed by connecting XAR bits 4 and 5 to pins 2 and 4 respectively. The commands DQA-DDD are ANDed together (NANDed and inverted) and the output connected to all the multiplexers as strobes at pins 1 and 15. When the ATAC reads a word, the XAR bits select the word and the strobe produces it during the microsecond when the PIO bus is available.

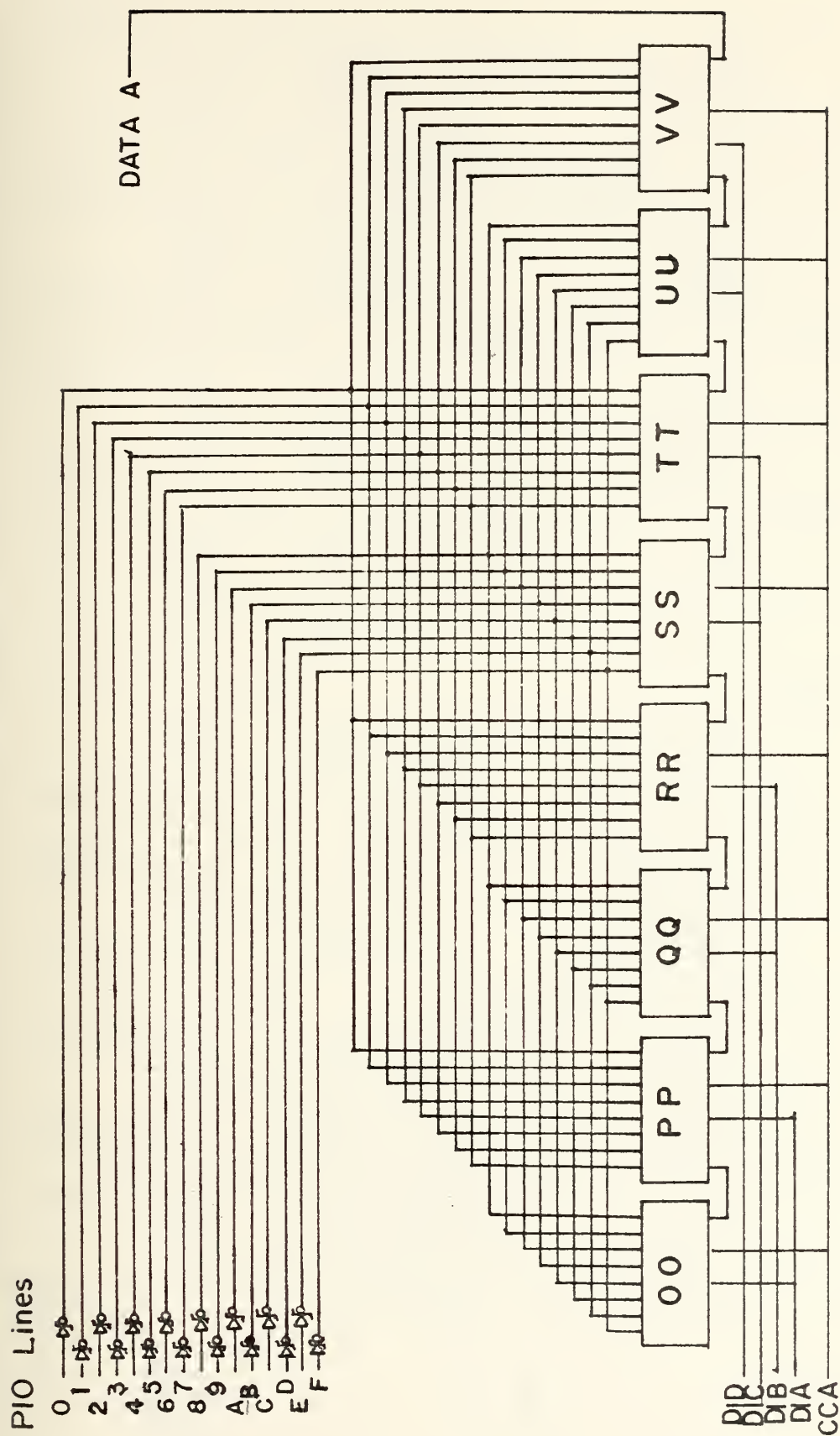


Figure 8
Input Register

P10 Lines

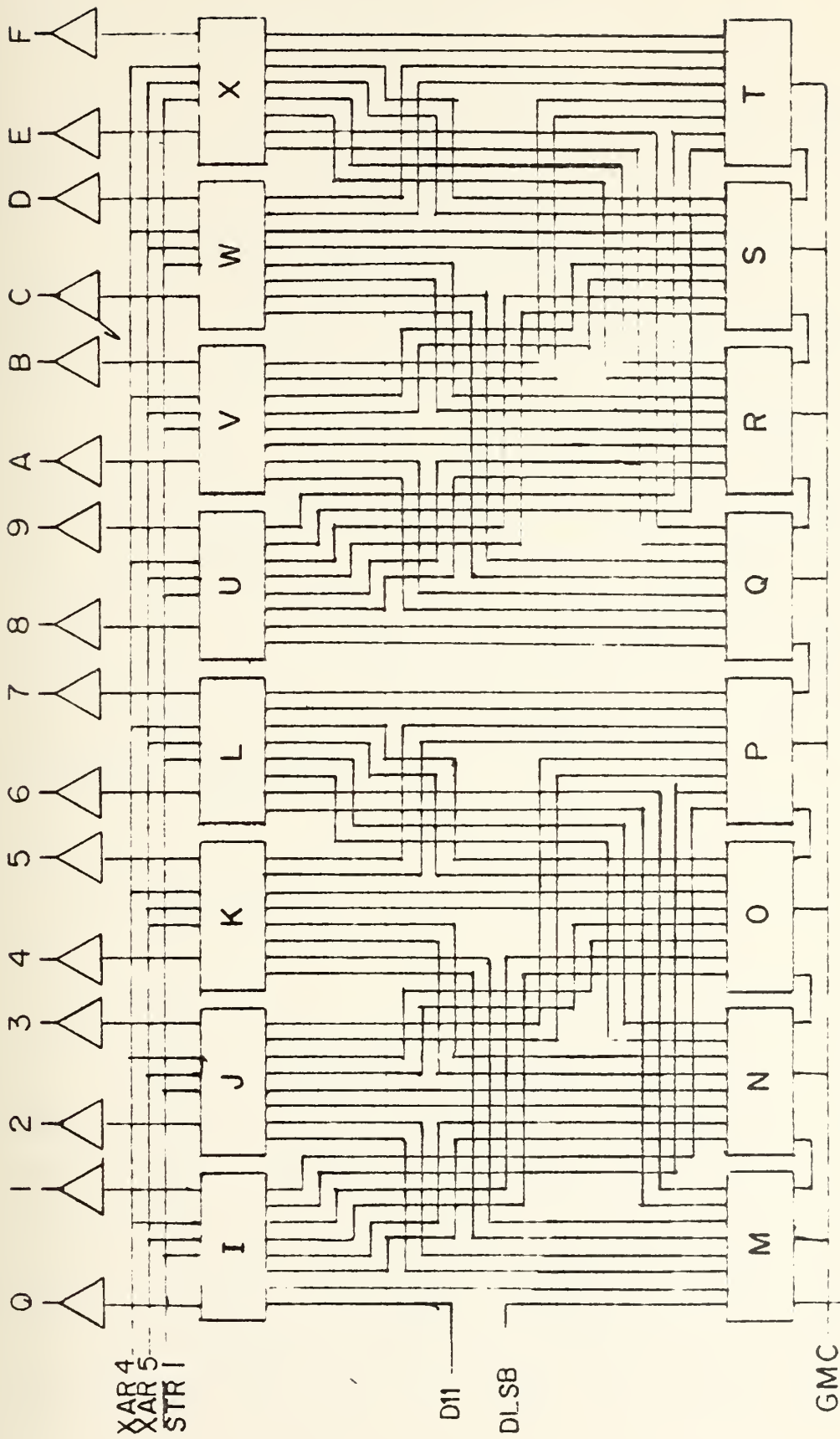


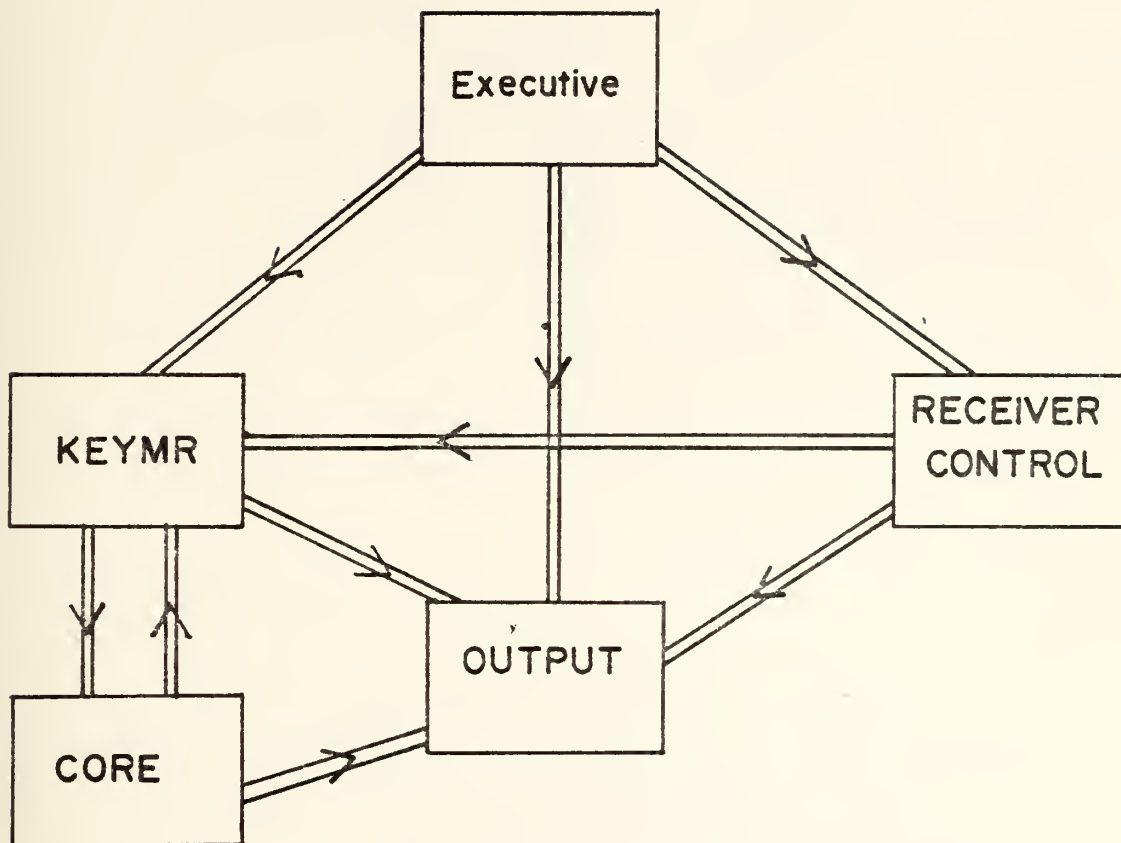
Figure 9
Output Register

V. THE PROGRAM

The ATAC program was written in two major sections; a system monitor and a control. The monitor is called the Main System and provides the operator the ability to program the ATAC from the operator's terminal. Receiver Control commands the interface and, therefore the receiver. Both programs were initially written prior to the construction of the interface, so many modifications were made using the Main System and its subroutines. After the interface was built and tested and the Receiver Control section modified to correctly control the tuning of the receiver, the complete program was saved on paper tape (Appendix C). Operation of the computer is discussed in Appendix B and a sample run can be found in Appendix F.

A. THE MAIN SYSTEM

The Main System section consists of a small executive and a group of interconnected subroutines (Figure 10). The executive provides a basis for the subroutines when the receiver control program is not being executed. It is these subroutines that control the input and output to the operator terminal. The input routine is called KEYMR and the output routine, OUTPUT. OUTPUT converts correctly-formatted computer words into ASCII and displays them on the




 = Subroutine Call

Figure 10
 ATAC Program Block Diagram

I. CORE Commands

- CO -- calls CORE from KEYMR.
- a. DU 'address' -- displays 80 memory locations beginning with 'address'.
 - b. DI 'address' -- displays the contents of memory location 'address'.
 - c. CH 'address' 'value' -- Replaces the contents of memory at 'address' with 'value'.
 - d. CS 'address' -- Beginning at 'address', the contents of memory are replaced with the values typed on the lines following the command. Exit is accomplished by command DN.
 - e. DN -- Returns execution to CORE if in CS, otherwise returns to calling routine.

II. Receiver Control Commands

- WJ -- Calls Receiver Control from the executive.
- a. 0 -- Set-up - Routine to input values for entry into Receiver.
 - b. 1 -- Displays set-up control word.
 - c. 2 -- Displays last control word sent to receiver.
 - d. 3 -- Displays last control received from receiver.
 - e. 4 -- Sends set-up control word to receiver.
 - f. 5 -- Routine to input scan variables and execute a scan.
 - g. 6 -- Receive and Display control word from the receiver.
 - h. 7 -- Exit program and return to caller.
 - i. 8 -- Reinitialize program as if entering.

Table IV
AFAC Program Commands

terminal. KEYMR does the reverse, and stores the input in a buffer for use by the caller. KEYMR and OUTPUT were programmed to accept and display only uppercase letters, numerals, and a small number of needed symbols. But, because of the method employed to convert ASCII to machine code, it was found that each lower case letter entered from the keyboard was automatically mapped into its respective upper case twin. This relieves the operator of the responsibility of using the shift key. A part of the KEYMR, called COPE, is available for use by the operator to display and/or change sections of memory. The four available commands in this routine and their functions are displayed in Table IV. Care must be taken not to change memory locations which are used by the Main System. This could result in complete erasure of the ATAC's memory. Without KEYMR, OUTPUT, and COPE, or routines similar to them, it would have been extremely difficult to perform any amount of troubleshooting or modification of the Receiver Control section.

B. RECEIVER CONTROL

This section of the system is a branch of the executive. Its main objective is to control both outputs and inputs of the interface from the operator's terminal. To assist those operators with little experience in this system, the Receiver Control section is equipped with uncomplicated

instructions and program safeguards. This produces almost foolproof operation but, it does so at the expense of program simplicity. Discussion of this section is separated into two parts. First a broad description of the complete section is discussed, followed by a detailed look at the two subroutines which interact with the interface.

When the Receiver Control program is entered, it performs five important actions. It initializes all necessary flags; enables the receiver and opens the MC gate; sends and receives a complete receiver word; and displays the instruction set to the operator. After this, it calls on KEYMR and waits for a command. When an input is delivered, the program checks its legality. If it is not a valid command, KEYMR is called again.

A valid command is a numeral between zero and eight (Table IV). These can be separated for discussion into three groups. The display group (0-3) inputs and exchanges information with the operator. The receiver group (4-6) performs operations with the receiver. The final group of commands (7-8) are used to exit or reinitialize the program. Group one has one input and three display commands. Command zero instructs the operator to input the parameters desired. It stores these parameters in memory in the display format, as opposed to control word format. Commands one, two, and three all display parameters. One displays the last parameters set-up by command zero. Two displays the last parameters sent to the receiver. Three displays the last

word received from the receiver. Commands seven and eight make up group three. Seven exits the program entirely and returns to the executive after disabling the receiver. Eight, on the other hand, returns the program to its beginning as if it had just been entered.

The remaining three commands are the most important. Group two commands control the actions of the interface. Command four converts the parameters set-up by command zero into control word format. It then calls the I/O subroutine described below, and outputs and inputs a receiver word. To merely receive a word from the receiver, command six is used. The program calls the input subroutine below and then exits to command three to display the parameters received. Command five scans a band of frequencies selected by the operator in search of a specified signal strength. All other parameters remain the same as those set-up by command zero.

With the exception of the instructions executed when entering and exiting Receiver Control, complete control of the interface and the receiver is resident in approximately forty computer instructions. These forty are grouped into the two subroutines WJR and WJS. WJS sends words to the receiver and WJR receives them. WJS loads the information and addresses to be sent to the receiver into the computer registers. The addresses are then matched to a word of data and sent to the interface input register. The routine now waits for the appropriate signal generated by RLP. When

this is received, a trigger command is sent to load the word into the receiver. At this point the routine checks the value of a counter. This test is to prevent the computer entering an infinite loop if either the interface or receiver is not turned on. If the test is unsatisfactory, the routine prints:

INFINITE LOOP
PLEASE CHECK RECEIVER AND INTERFACE

and reverts to operator control. If the test is satisfactory, the subroutine automatically continues to WJR. WJR loads another set of addresses into the computer registers. Here, a short wait for the RLP signal is necessary before any action is taken. The MC gate is closed immediately upon receipt of this signal. The receiver word is then loaded into the ATAC by outputting the address on the XAP lines and reading the data on the PIO lines. When the complete word is received, the MC gate is opened. At this point it is necessary to test for command six. This test determines whether the computer is sending and receiving or only receiving. If the execution of both WJS and WJR is being performed, a comparison between the word sent and the word received is necessary. This comparison is skipped if the computer is only executing WJR (command six). The first three control words sent by WJS and received by WJR are used for this comparison, when it is performed. If

any words differ, the computer returns to WJS to repeat the cycle until one of two conditions are met: either the words match or the WJS counter test discussed earlier fails. If the words match, WJP continues on to convert the received control words into the display format and then returns to the caller.

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VI. RECOMMENDATIONS

The system as it stands now is but a beginning. Additions and modifications for future work should include; A/D converters for the receiver outputs; Morse and/or teletype decoders; and an expansion of the computer program. Implementation of either of the first two implies the third. There are some operator assistance program modifications that need to be made. The two that come immediately to mind are (1) a method to abort the scan routine from the operator's console, and (2) the ability to change individual parameters in addition to the set-up command already located in the program. Addition of the A/D converters implies a program increase to decode and process this new data. Switching routines and probably some hardware will be needed for the decoders. The capabilities of the system are limited only by the abilities of the operator and programmer.

VII. CONCLUSION

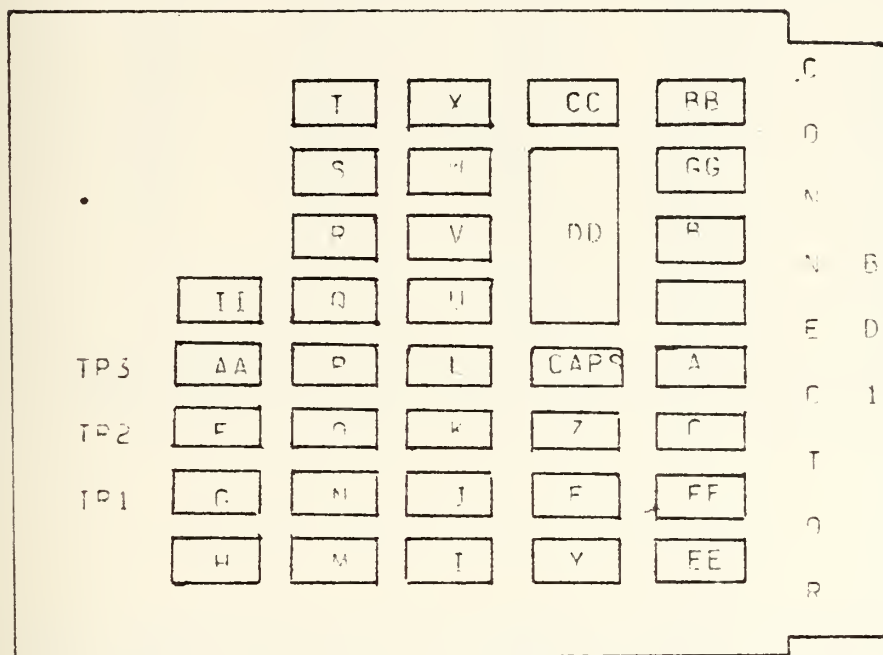
As long as the computer requires only that data obtained from the receiver's word, the interface is flexible enough to provide reliable results. At this time there are no known "bugs" in either the interface or the program. Both have been thoroughly tested to provide the operator with the most dependable system possible.

APPENDIX A

INTERFACE WIRING

A. Board 1

Integrated circuit locations (from Top of board).



Integrated Circuit

pin	A	B	C	F	F	G	H
	8820	8820	8830	7476	7404	7400	74157
1	PD1-M	PD1-K	C-2/Z-3	VCC	M-3	BD2-E	DD-14
2	nc	nc	C-1/C-3	DD-8	H-3	Y-9	II-14
3	BD1-L	BD1-J	C-2/C-4	DD-15	A-6/Y-8	F-11	F-2
4	nc	nc	C-3	VCC	G-5	E-11	I-6
5	nc	nc	BD1-F	VCC	AA-6	F-4	nc
6	F-3/Y-8	M-1	BD1-H	VCC	G-12	F-9	nc
7	GRD	GRD	GRD	DD-7	GRD	GRD	GRD
8	nc	nc	nc	DD-6	I-8	nc	nc
9	nc	nc	nc	VCC	G-6	nc	nc
10	nc	nc	nc	nc	II-3	nc	nc
11	nc	nc	nc	G-4	G-3	F-13	nc
12	nc	nc	nc	VCC	I-15	F-6	nc
13	nc	nc	nc	GRD	G-11	DD-14	GRD
14	VCC	VCC	VCC	nc	VCC	VCC	VCC
15	XXXXXX	XXXXXX	XXXXXX	PD1-Y	XXXXXX	XXXXXX	XXXXXX
16	XXXXXX	XXXXXX	XXXXXX	VCC	XXXXXX	XXXXXX	XXXXXX

Integrated Circuit

pin	I	J	K	L	M	N
	7214	7214	7214	7214	74164	74164
1	X-15	I-15/J15	J-15/K15	K-15/L15	B-6/M-2	M-13/N-2
2	DD22/J-2	I-2/K-2	J-2/L-2	K-2/U-2	M-1	N-1
3	S-3	S-5	S-10	S-12	F-1	U-6
4	Q-3	Q-5	Q-10	Q-12	I-10	U-10
5	Q-3	Q-5	Q-10	Q-12	J-6	V-6
6	H-4	M-5	M-10	M-12	J-10	V-10
7	EE-1	FE-5	EF-11	FF-1	GRD	GRD
8	GRD	GRD	GRD	GRD	M-8	M-8/O-8
9	EE-3	FE-9	EF-13	FF-3	VCC	VCC
10	M-4	M-6	M-11	M-13	K-6	W-6
11	Q-4	Q-6	Q-11	Q-13	K-10	W-10
12	Q-4	Q-6	Q-11	Q-13	L-6	X-6
13	S-4	S-6	S-11	S-13	L-10	X-10
14	DD23/J14	K-14/I14	J-14/L14	K-14/U14	VCC	VCC
15	F-12/J-1	J-1/K-1	K-1/L-1	L-1/U-1	XXXXXXXXXX	XXXXXXXXXX
16	VCC	VCC	VCC	VCC	XXXXXXXXXX	XXXXXXXXXX

pin	U	P	Q	R	S	T
	74164	74164	74164	74164	74164	74164
1	N-13/O-2	O-13/P-2	P-13/Q-2	Q-13/R-2	R-13/S-2	S-13/T-2
2	Q-1	P-1	Q-1	R-1	S-1	T-1
3	I-5	U-5	I-4	U-4	I-3	U-3
4	I-11	U-11	I-12	U-12	I-13	U-13
5	J-5	V-11	J-4	V-4	J-3	V-3
6	J-11	V-11	J-12	V-12	J-13	V-13
7	GRD	GRD	GRD	GRD	GRD	GRD
8	N-8/P-8	O-8/Q-8	P-8/R-8	Q-8/S-8	R-8/T-8	S-8/F-8
9	VCC	VCC	VCC	VCC	VCC	VCC
10	K-5	W-5	K-4	W-4	K-3	W-3
11	K-11	W-11	K-12	W-12	K-13	W-13
12	L-5	X-5	L-4	X-4	L-3	X-3
13	L-11	X-11	L-12	X-12	L-13	X-13
14	VCC	VCC	VCC	VCC	VCC	VCC

Integrated Circuit

	U	V	W	X	Y	Z
pin	7214	7214	7214	7214	556	555
1	L-15/U15	U-15/V15	V-15/W15	W-15/X15	Y2/Tp-1A	GRD
2	L-2/V-2	U-2/W-2	V-2/X-2	W-2	Y-1/HH-6	PD1-E
3	T-3	T-5	T-10	T-12	HH-5	C-1
4	P-3	R-5	P-10	R-12	VCC	VCC
5	P-3	P-5	P-10	P-12	BD1C/II1	HH-1
6	N-3	N-5	N-10	N-12	Y-9	HH-2/Z-7
7	FF-5	FF-11	GG-1	GG-5	GRD	Z6/Tp-3A
8	GRD	GRD	GRD	GRD	A-6/F-3	VCC
9	FF-9	FF-13	GG-3	GG-9	Y-6	XXXXXXXXXX
10	N-4	N-6	N-11	N-13	VCC	XXXXXXXXXX
11	P-4	P-6	P-11	P-13	HH-4	XXXXXXXXXX
12	R-4	R-6	R-11	R-13	Y-13/HH4	XXXXXXXXXX
13	T-4	T-6	T-11	T-13	Y12/Tp2A	XXXXXXXXXX
14	L-14/V14	U-14/W14	V-14/X14	W-14	VCC	XXXXXXXXXX
15	U-1/V-1	V-1/W-1	W-1/X-1	X-1/[-1	XXXXXXXXXX	XXXXXXXXXX
16	VCC	VCC	VCC	VCC	XXXXXXYYXX	XXXXXXXXXX

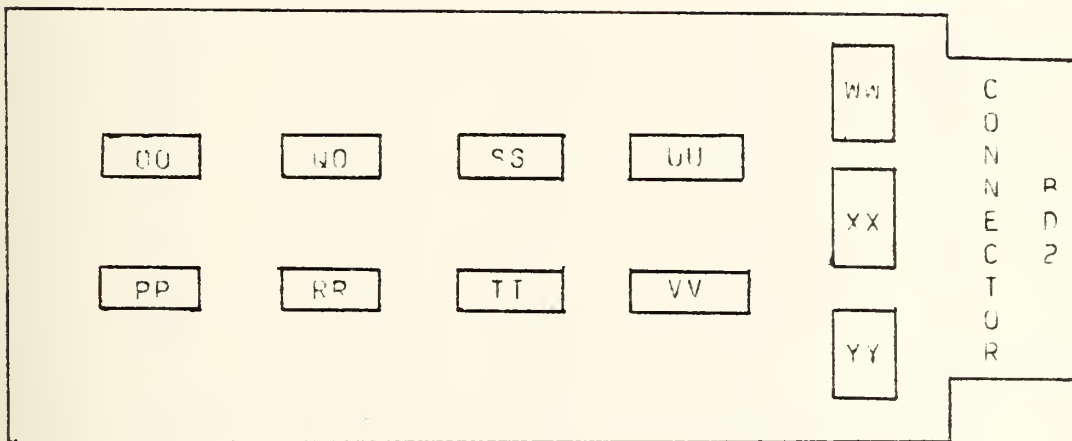
	AA	BB	CC	EE	FF	GG	HH	II
pin	7420	74s04	74s04	7407	7407	7407	CAPS	7476
1	DD-10	CC-6	BD1-17	T-7	L-7	W-7	Z-5	Y-5
2	DD-11	DD-18	DD-23	BD1-1	BD1-7	PD1-13	Z-6	VCC
3	nc	BD1-21	nc	I-9	L-9	W-9	Y-11	F-10
4	DD-9	BB-5	nc	BD1-2	BD1-8	PD1-14	Y-12	VCC
5	DD-13	BB-4	BD1-T	J-7	U-7	X-7	Y-3	nc
6	F-5	DD-19	BB-1	BD1-3	BD1-9	BD1-15	nc	nc
7	GRD	GRD	GRD	GRD	GRD	GRD	Y-2	nc
8	nc	DD-20	nc	BD1-4	BD1-10	BD1-16	GRD	nc
9	nc	BD1-20	nc	J-9	U-9	X-9	GRD	nc
10	nc	DD-21	nc	BD1-5	BD1-11	nc	GRD	nc
11	nc	BD1-19	nc	K-7	V-7	nc	GRD	nc
12	nc	DD-22	nc	BD1-6	BD1-12	nc	GRD	nc
13	nc	BD1-18	nc	K-9	V-9	nc	GRD	GRD
14	VCC	VCC	VCC	VCC	VCC	VCC	GRD	H-2
15	XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	nc
16	XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	GRD

Integrated Circuit

		DD	
		74154	
pin		pin	
1	RD1-P	13	AA-5
2	RD1-X	14	G-13/H-1
3	RD1-V	15	nc
4	RD1-V	16	nc
5	RD1-U	17	F-3
6	E-8	18	BR-2
7	E-7	19	BR-6
8	E-2	20	GR-8
9	AA-4	21	BR-10
10	AA-1	22	BR-12/I-2
11	AA-2	23	CC-2/I-14
12	GRD	24	VCC

II. Board 2

Integrated Circuit Locations (from Top of board)



Integrated Circuit

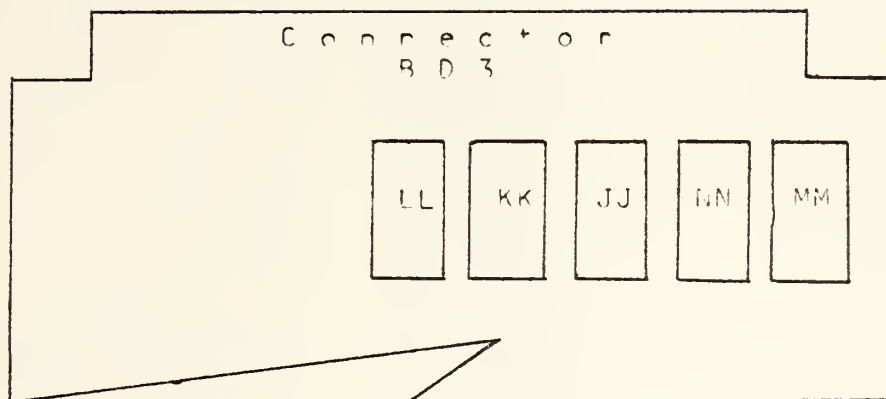
pin	00	PP	QQ	RR	SS	TT
1	BD2-A	BD2-A	BD2-B	BD2-B	BD2-C	BD2-C
2	GRD	GRD	GRD	GRD	GRD	GRD
3	WW-2	YY-6	WW-2	YY-6	WW-2	YY-6
4	WW-12	YY-4	WW-12	YY-4	WW-12	YY-4
5	WW-4	YY-2	WW-4	YY-2	WW-4	YY-2
6	WW-10	YY-10	WW-10	YY-10	WW-10	YY-10
7	nc	nc	nc	nc	nc	nc
8	GRD	GRD	GRD	GRD	GRD	GRD
9	PP-10	QQ-10	PP-10	SS-10	TT-10	UU-10
10	VCC	QQ-9	PP-9	QQ-9	RR-9	SS-9
11	XX-2	XX-4	XX-2	XX-4	XX-2	XX-4
12	XX-12	XX-6	XX-12	XX-6	XX-12	XX-6
13	WW-8	XX-8	WW-8	XX-8	WW-8	XX-8
14	WW-6	YY-12	WW-6	YY-12	WW-6	YY-12
15	BD2-21	BD2-21	BD2-21	BD2-21	BD2-21	BD2-21
16	VCC	VCC	VCC	VCC	VCC	VCC

pin	UU	VV	WA	YX	YY
1	BD2-D	BD2-D	BD2-17	BD2-10	BD2-4
2	GRD	GRD	QQ-3 *	QQ-11 *	PP-5 *
3	WW-2	YY-6	BD2-15	BD2-9	BD2-3
4	WW-12	YY-4	QQ-5 *	PP-11 *	PP-4 *
5	WW-4	YY-2	BD2-13	BD2-8	BD2-2
6	WW-10	YY-10	QQ-14 *	PP-12 *	PP-3 *
7	nc	nc	GRD	GRD	GRD
8	GRD	GRD	QQ-13 *	PP-13 *	nc
9	VV-10	BD2-K	BD2-12	BD2-7	nc
10	TT-9	UU-9	QQ-6 *	nc	PP-6 *
11	XX-2	XX-4	BD3-14	nc	BD2-5
12	XX-12	XX-6	QQ-4 *	QQ-12 *	PP-14 *
13	WW-8	XX-8	BD2-16	BD2-11	BD2-6
14	WW-6	YY-12	VCC	VCC	VCC
15	BD2-21	BD2-21	XXXXXXXXXX	XXXXXXXXXX	XXXXXXXXXX
16	VCC	VCC	XXXXXXXXXX	XXXXXXXXXX	XXXXXXXXXX

* - bus connection - only first connection shown

C. Board Three

Integrated circuit locations (from Top of board)



Integrated Circuit

	JJ	KA	LL	NN	NN
pin	74157	7476	8830	74126	8820
1	BD3-1	VCC	LL-2/JJ-7	BD3-1	BD3-5
2	KK-15	BD3-11	LL-1/LL-3	BD3-17	nc
3	BD3-6	BD3-12/20	LL-2/LL-4	BD3-16	BD3-4
4	LL-10	nc	LL-3	JJ-12	nc
5	BD3-8	VCC	BD3-7	GRD	nc
6	BD3-9	nc	BD3-10	BD3-16	MM-a
7	LL-1	nc	GRD	GRD	GRD
8	GRD	nc	BD3-19	BD3-2	nc
9	BD3-13	nc	BD3-18	NN-8	nc
10	BD3-14	nc	LL11/JJ-4	BD3-1	nc
11	nc	nc	LL12/LL10	BD3-3	nc
12	MM13/MM-4	nc	LL13/LL11	MM-a	nc
13	GRD	GRD	LL-12	JJ-12	nc
14	KK-15	nc	VCC	VCC	VCC
15	GRD	JJ-2/JJ14	XXXXXXXXXX	XXXXXXXXXX	XXXXXXXXXX
16	VCC	nc	XXXXXXXXXX	XXXXXXXXXX	XXXXXXXXXX

D. Connectors

Circuit Board Edge-connectors

	RD1	RD2	RD3
1	EE-2/RD2-10/CN1-2	GRD	SW1/JJ-1/MM-10
2	EE-4/RD2-11/CN1-3	YY-5/RD1-13	MM-8/RD2-21
3	EE-6/RD2-12/CN1-4	YY-3/RD1-14	MM-11/CN3-1
4	EE-8/RD2-13/CN1-5	YY-1/RD1-15	NN-2/CN2-2
5	EE10/RD2-17/CN1-6	YY-11/RD1-16	NN-1/CN2-3
6	EE12/RD2-16/CN1-7	YY-13/RD1-12	JJ-3/RD1-Y
7	FF-2/RD2-15/CN1-8	XX-9/RD1-11	LL-5/CN2-10
*8	FF-4/RD2-14/CN1-9	XX-5/RD1-10	JJ-5/CN3-2
9	FF-6/RD2-9/CN1-10	XX-3/RD1-8	JJ-6/RD2-K
10	FF-8/RD2-8/CN1-11	XX-1/RD1-1	LL-6/CN2-11
11	FF10/RD2-7/CN1-12	XX-13/RD1-2	KK-2/CN3-3
12	FF12/RD2-6/CN1-13	WW-9/RD1-3	KK-3/CN3-4
13	GG-2/RD2-2/CN1-25	WW-5/RD1-4	JJ-9/RD1-E
14	GG-4/RD2-3/CN1-24	WW-11/RD1-8	JJ-10/RD1-P
15	GG-6/RD2-4/CN1-23	WW-3/RD1-7	IJ-11/CN3-5
16	GG-8/RD2-5/CN1-22	WW-13/RD1-6	nc
17	CC-1/CN1-11	WW-1/RD1-5	nc
18	PP-13/CN1-17	nc	LL-9/CN2-12
19	PP-11/CN1-19	nc	LL-8/CN2-11
20	BP-9/CN1-16	nc	KK-3/RESET
21	BP-3/CN1-20	DD-15/RD3-2	nc
22	nc	GRD	VCC
A	GRD	DD-1/RD1-X	GRD
B	nc	GG-1/RD1-W	nc
C	II-14/CN3-6	SS-1/RD1-V	nc
D	nc	UU-1/RD1-U	nc
E	7-2/RD3-13	nc	nc
F	C-5/CN2-9	nc	nc
H	C-6/CN2-8	nc	nc
J	B-3/CN2-7	nc	nc
K	B-1/CN2-6	nc	nc
L	A-3/CN2-5	nc	nc
M	A-1/CN2-4	nc	nc
N	nc	nc	nc
P	DD-1/RD3-14	nc	nc
R	nc	nc	nc
S	nc	nc	nc
T	CC-5/CN1-14	nc	nc
U	DD-5/RD2-D	nc	nc
V	DD-4/RD2-C	nc	nc
W	DD-3/RD2-B	nc	nc
X	DD-2/RD2-A	nc	nc
Y	E-15/RD3-6	nc	nc
Z	VCC	nc	nc

Cabinet Connectors

pin:	CN1	CN2	CN3
1	GRD	GRD	BD3-3 "CCK"
2	BD1-1 "PIO 0"	BD3-4 "CC - "	BD3-8 "DATA K"
3	BD1-2 "PIO 1"	BD3-5 "CC + "	BD3-11 "KAO"
4	BD1-3 "PIO 2"	BD1-M "MC - "	BD3-12 "KAF"
5	BD1-4 "PIO 3"	BD1-L "MC + "	BD3-15 "TRK"
6	BD1-5 "PIO 4"	BD1-K "DO - "	BD1-3 "PLD"
7	BD1-6 "PIO 5"	BD1-J "DO + "	nc
8	BD1-7 "PIO 6"	BD1-H "TR - "	nc
9	BD1-8 "PIO 7"	BD1-F "TR + "	nc
10	BD1-9 "PIO 8"	BD3-7 "DI - "	nc
11	BD1-10 "PIO 9"	BD3-10 "DI + "	nc
12	BD1-11 "PIO 10"	BD3-19 "AD - "	nc
13	BD1-12 "PIO 11"	BD3-18 "AD + "	nc
14	BD1-T "IOU"	nc	GRD
15	nc	nc	nc
16	BD1-17 "XAP 4"	nc	nc
17	BD1-18 "XAP 5"	nc	nc
18	BD1-20 "XAP 9"	nc	nc
19	BD1-19 "XAP 8"	nc	nc
20	BD1-21 "XAP 13"	nc	nc
21	nc	nc	nc
22	BD1-16 "PIO-15"	nc	nc
23	BD1-15 "PIO-14"	nc	nc
24	BD1-14 "PIO-13"	nc	nc
25	BD1-13 "PIO-12"	nc	nc

E. Discrete Components

Capacitors

.01 uF	HH-1/HH-14
.2 uF	HH-2/HH-13
.20 uF	HH-3/HH-12
.01 uF	HH-4/HH-11
.01 uF	HH-5/HH-10
.47 uF	HH-7/HH-8

Resistors

Trimmer			
	1	2	3
A	Y-1	Y-13	Z-7
B	VCC	VCC	VCC
C	VCC	VCC	VCC

APPENDIX B ATAC OPERATING INSTRUCTIONS

Power Up

Turn on front panel power then turn on power supplies.

Power Down

'Halt'

'Master Clear'

Power off to supplies, power off to control panel.

Run Program

'Master Clear'

Dial 'IMR'

'AUX REG'

'ENTER' (associated with AUX REG)

'MEMORY'

Set start address +1 in keyboard (Hexadecimal)

'PCP'

'ENTER' (associated with PCP)

'RUN'

Stop a Program

'HALT'

Read Memory (from front panel)

'HALT'

Set desired address in key board

Select 'MAR'

'ENTER' (associated with MAR)

'INC' (increment)

'DEC' (decrement)

Address is displayed above MAR key, data is displayed in red LEDs above MEMORY key.

Use INC or DEC as necessary to arrive at memory location desired.

Write into Memory (from front panel)

'HALT'

Set address desired as described in Read Memory.

Set desired data into keyboard

'ENTER' (associated with MEMORY)

Value in keyboard will be entered into either Memory (MEMORY) or A computer Register (FILE).

Bootstrap Load (paper tape)

'HALT'

'MASTER CLEAR'

'AUX REG'

Dial 'IMR'

'ENTER' (associated with AUX REG)

'MEMORY'

Set 0001 in keyboard

(0001 = Load, 0002 = Verify only)

'RUN'

At end of tape check program status lights (red LEDs
below PCR and MAR pushbuttons)

0000 = Load good

FFFE = Parity error

FFFD = Verify error

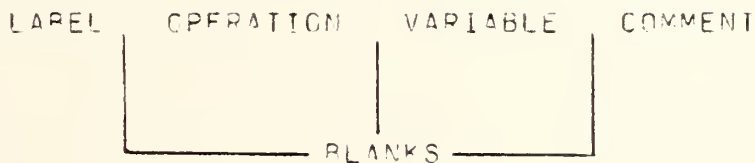
APPENDIX C

ATAC PROGRAM ASSEMBLY

Assembly of a program is divided into five parts; writing, producing absolute deck on IBM 360, conversion of absolute deck into ATAC format, punching paper tape, and loading ATAC.

A. Writing the program.

Programs for the ATAC must be written in the assembly language described in ATAC manuals Volumes One, and Eight. The finished program must be placed on cards for the IBM 360 in the following format:



B. Producing an absolute deck

The first step is to load the assembler on to the IBM 360 from magnetic tape. This is done by executing program A in Appendix E. This transfers the program from tape to disk and saves it for one year. Once the assembler is stored the

following cards placed in the front of a program written following the instructions in I above will produce an absolute deck and a print-out of the program.

```
//ATACASSM JOB (0729,0194,0052),'CCH ATAC ASSEM,',TIME=1
//ASSEM      EXEC PGM=APSS,REGION=220K
//STEPLIB DD  DSN=S0729.ATAC.0NF,UNIT=3330,
//              VOL=SER=DISK02,DISP=SHR
//FT06F001 DD  SYSCUT=A
//FT07F001 DD  SYSCUT=B
//FT05F001 DD  DDNAME=SYSIN
//FT08F001 DD  UNIT=SYSDA,SPACE=(CYL,1)
//FT09F001 DD  UNIT=SYSDA,SPACE=(CYL,(7,2)),
//              DCR=(RECFM=VRS,BLKSIZE=7180,LRECL=92)
//FT10F001 DD  UNIT=SYSDA,SPACE=(CYL,(7,2)),
//              DCR=(RECFM=VRS,BLKSIZE=4204,LRECL=42)
//FT20F001 DD  UNIT=SYSDA,SPACE=(CYL,(7,2)),
//              DCR=(RECFM=VRS,BLKSIZE=2004,LRECL=500)
//SYSPPRINT DD  SYSCUT=A
//SYSIN      DD  *
$JOB
$ASSEM
      IDT    ATAC
```

(place written program here.)

```
      END
$BASE
$LOAD    P
$END
```

The absolute deck is in the form:

```
0500169c0009adbc3109bc9c3109c8bc7109c09c7109d8b60309bbd932/
                                                    /e10100009c015a
05101609f49c0109f6ed0008aee1010a02ed000230e10109f7ed0007ae/
                                                    /c1070509201258
```

which must be translated for the ATAC. The memory location of the first word is located in the first four columns.

Columns five and six contain the number of word fields on the card. The assembled program is located in columns 7 - 70. The remaining two columns are parity.

C. Conversion

The absolute deck received from the IBM 360 is loaded into the PDP-11. After the data from the cards is checked, the conversion program (convert 'filename' 'filename') can be executed. (Program C in Appendix F)

D. Punching Paper Tape

This code must then be transferred to the PDP-11 (A) where a paper tape can be punched. Here, the command to punch a tape is:

```
cat 'filename' >/dev/ptp
```

E. Loading the AT10

In order to load a tape the RS232 connector must be connected to the Paper Tape reader and the reader set to 1200 baud. The tape is loaded by following the instructions in Appendix B.

APPENDIX D

SAMPLE ATAC OUTPUT

Operator inputs are underlined.

Operator Display	*Comments
EXEC	*Executive echos
+ <u>JDKDKJFJJJnmun</u>	*entries other than
JDKDKJFJJJNMUH	*commands
EXEC	
+ <u>CO</u>	*Entry into CORE
CORE	
+ <u>CH 0F00 0900</u>	*Location 0F00
0F00 0900	*changed to 0900
CORE	
+ <u>DI 0F00</u>	
0F00 0900	
CORE	
+ <u>CS 0F00</u>	*Locations 0F00 to 0F03
+ <u>0256</u>	*changed
+ <u>0123</u>	
+ <u>4567</u>	
+ <u>DO</u>	*completion of change
0F00 0256	
0F01 0123	
0F02 4567	
CORE	
+ <u>DO</u>	*Exit from CORE
+ <u>WJ</u>	*Entry into Receiver
0=SET-UP	*Control
1=DISPLAY TENTATIVE	
2=DISPLAY CONTROL	
3=DISPLAY RECEIVED	
4=ENTER TENTATIVE	
5=SCAN	

6=RECEIVE CONTROL

7=DONE

8=REINITIALIZE

RECEIVER CONTROL

+0

FREQ(HZ)

+1240000

DETECT MODE

0=AM

1=FM

2=BFO FIXED

3=BFO VARIABLE

4=ISB

5=USB

6=LSB

7=AM-NL

+0

GAIN MODE

0=HOLD AGC

2=NORMAL AGC

3=MANUAL AGC

+0

IF BANDWIDTH

1=500 HZ

2=2 KHZ

3=4 KHZ

4=8 KHZ

+4

RF GAIN

(PERCENTAGE)

+88

RECEIVER CONTROL

+1

FREQ = 1240000 HZ

GAIN MODE = HOLD AGC

IF BANDWIDTH = 2 KHZ

DETECT MODE = AM

BFO FREQ = 455000 HZ

RF GAIN = 88%

RECEIVER CONTROL

+2

FREQ = 550000 HZ
GAIN MODE = NORMAL AGC
IF BANDWIDTH = 8 KHZ
DETECT MODE = AM
BFO FREQUENCY = 455000 HZ
RF GAIN = 85%

RECEIVER CONTROL

+3

FREQ = 550000 HZ
GAIN MODE = NORMAL AGC
IF BANDWIDTH = 8 KHZ
DETECT MODE = AM
BFO FREQUENCY = 455000 HZ
RF GAIN = 85%
SIGNAL STRENGTH = 66%

RECEIVER CONTROL

+4

RECEIVER CONTROL

+5

SCAN
START FREQ IN HZ

+1000000

END FREQ IN HZ

+1008000

FREQ INCREMENT IN HZ

+1000

SIGNAL STRENGTH %

+67

FREQ = 1001000
GAIN MODE = HOLD AGC
IF BANDWIDTH = 8 KHZ
DETECT MODE = AM
BFO FREQUENCY = 455000 HZ
RF GAIN = 88%
SIGNAL STRENGTH = 72%

RECEIVER CONTROL

+7

EYEC

+

*Exit from
*Receiver Control

APPENDIX E CONVERSION PROGRAMS FOR THE ASSEMBLER

A. This program is run on the IBM-360 to transfer the ATAC assembler from tape ATT-006 to Disk and stores it there for one year.

```
// (GREEN JOB CARD)
//SYSPRINT DD   SYSOUT=A
//SYSUT1 DD    UNIT=SYSDA,SPACE=(TRK,(40),,CONTIG)
//DA1 DD      UNIT=2314,DSN=S0729.ATAC.ONE,
//            SPACE=(TRK,(50,10,10),,CONTIG),
//            DISP=(NEW,KEEP),VOL=SER=SPOOL3
//T1TAPE DD UNIT=(2400,,DFFER),DISP=(NEW,PASS),
//            LABEL=(3,SL,,IN),
//            DCR=(DCR=2,BLKSIZE=800,LRECL=80,RECFM=FB),
//            VOL=SER=ATT006
//SYSIN DD      *
//              COPY   PDS=ATT.APSS.LOADLIB,TO=2314=SPOOL3,
//                      FROMD=T1TAPE,FROM=2400=(ATT006,3),
//                      RENAME=S0729.ATAC.ONE

/*
//BUILD EXEC PGM=IEWL,REGION=150K,
//      PARM='DVLY,XPEF,LET,LIST,SIZE=(256K,20480)'
//SYSPRINT DD   SYSOUT=A
//LIBRARY DD DSN=S0729.ATAC.ONE,UNIT=2314,VOL=SER=SPOOL3,
//          DISP=SHR
//SYSLIB DD DSN=SYS1.FORTLIB,DISP=SHR
//SYSLMOD DD DSN=S0729.ATAC.ONE,
//          UNIT=3330,VOL=SER=DISK02,
//          DISP=(NEW,KEEP),LABEL=PETPD=360,
//          SPACE=(CYL,(5,1,2),RLSE)
//SYSUT1 DD UNIT=SYSDA,SPACE=(TRK,(19,19),,CONTIG),
//          SEP=SYSLMOD
//SYSLIN DD      *
//      INCLUDE LIBRARY(PVHDL)
//      CHANGE MSIM(IHESAPD)
//      INCLUDE LIBRARY(APSSMON)
//      INCLUDE LIBRARY(MSIM4,ASEM5,SIM16A,SIMTR1,SIMIO1,GUL)
//      INCLUDE LIBRARY(XPLMON)
//      OVERLAY A1
//      INSERT MSIMUL,*MSIMUL A,IHENTRY,IHESAP
//      INSERT MINT,IN,OUT
//      INSERT IHEDBN,IHEXTD
```



```

INSERT IHERSM,IHECSM
INSERT IHERSK,IHFIOX,IHEIOP,IHEDIO,IHEDOB
INSERT IHEDIB,IHEDOA,IHEIOB
INSERT IHEIOA,IHEOCL
INSERT IHERSD,IHEBSF
INSERT IHEJXS
INSERT IHEOSD,IHEOST,IHERST
INSERT IHEVPF,IHEDMA,IHEVER
INSERT IHEDNC,IHEVFD,IHEVFA,IHEVPD,IHEVPR,IHEVSC
INSERT IHEVSD,IHEVFE,IHEDCN,IHEUPB
INSERT IHEVFC,IHEVPE,IHEVPG,IHEVOB,IHEVGC
INSERT IHEABN,IHEIOO,IHEIOF,IHEPRT,IHEVQA,IHESPR
INSERT IHEREG,IHEPR,IHESI7
INSERT MISEF
OVERLAY A1
INSERT ASSEM,REWIND,REW72,DSKOUT,CARDIN,DISKIN,ERPRT,PRIADD
INSERT WRDATA,PRICOM,PRINOP,RTITEX,REFTIT,PREF,EPTIT
OVERLAY A1
INSERT PARMRD,PRESTM
OVERLAY A1
INSERT SMLTR,HPMTR,STRISM,TRAGE
INSERT RDCPD,ABNPMT,ARTHER,TRACE,HGRAY,HGRAMI,HGRAMS
INSERT IQINIT,ACTIVE,STMTIM
INSERT DEVDTA,ACT,TIME,INT,RAND,DEADT,DEBUG
OVERLAY A2
INSERT LEVEL,DMAIOI,DMAIOA,DMAIOD,RIOIO
INSERT REMACT,DMA,DMAIM,RIO,RIOIM,RIOINT,INTOLY,DMAINT
INSERT DTRAN,PUTACT,RANDOM
OVERLAY A1
INSERT HGPRNT
OVERLAY A1
INSERT LOADER
OVERLAY A1
INSERT LINK,ENTEXT,SILH
OVERLAY A1
INSERT PLATAC,TOPACK
OVERLAY $OBJECT(REGION)
INSERT OBJECT,INIT,LIB,RCALPH,RCHEX,RCINT
INSERT MDATE
OVERLAY $DUMP(REGION)
INSERT SMDUMP,PAGE
ENTRY MAIN
NAME APSS
/*
//          EXEC PGM=IEBCOPY
//SYSPRINT DD   SYSCUT=A
//SYSUT1  DD   DISP=SHR,UNIT=2314,VOL=SER=SP00L3,
//          DSN=S0729.ATAC.ONE
//SYSUT2 DD   DISP=(NEW,PASS),UNIT=3330,VOL=SER=DISK02,
//          DSN=S0729.ATAC.TWO,

```



```

//          SPACE=(13030,(61,0,14),RLSE),
//          DCB=(RECFM=U,BLKSIZE=13030),
//          ,LABEL=RFIPD=360
//SYSUT3 DD UNIT=SYSDA,SPACE=(TRK,(20,5))
//SYSUT4 DD UNIT=SYSDA,SPACE=(TRK,(20,5))
//SYSIN DD *
COPY OUTDD=SYSUT2,INDD=SYSUT1

```

d. This program converts the IBM-360 absolute deck into correct format for the ATAC.

```

main (argc, *argv)
    int argc;
    char *argv [1];
    {register crctr, index, index;
    int stchr;
    int tcopy [731];
    struct bufin
        {int fides;
        int nleft;
        char *nextp;
        char *buffs [512];
        } bufin, bufot, *pnt1, *pnt2;
    stchr = 020;
    if (argc != 3)
        {printf ("Calling arguments are incorrect#");
        exit (0);
        }
    bufin.fides = open (argv [1], 0);
    if (bufin.fides < 0)
        {printf ("Cannot open %s#", argv [1]);
        exit (0);
        }
    pnt1 = &bufin.fides;
    bufot.fides = creat (argv [2], 0777);
    if (bufot.fides < 0)
        {printf ("Cannot open %s#", argv [2]);
        exit (0);
        }
    pnt2 = &bufot.fides;
    outc (stchr, pnt2);
    while (crctr >= 0 && index <= 72)
        tcopy [index++] = (crctr =getc (pnt1));
    index -- 3;
    index = 0;
    while (index < 4 && index < index)

```



```

       putc (tmpary [jindex++], pnter2);
index = index + 2;
while (cncrtr >= 0)
    {while (jindex < index)
        {if (tmpary [jindex] == '#')
            jindex++;
        else
            putc (tmpary [jindex++], pnter2);
        }
    index = 0;
    while (cncrtr >= 0 && index <= 72)
        tmpary [index++] = (cncrtr =getc (pnter1));
    index -= 3;
    jindex = 0;
}
putc (stchr, pnter2);
fflush (pnter2);
close (bufin.flcse);
close (bufot.flcse);
}

```

C. The following program executes the program above and converts the output into the correct code.

```

atrac $1 $2
if ! -r $2 exit
mv $2 temp2
tr "[0*]" "[040*]" <temp2 >temp1
tr "[1*]" "[001*]" <temp1 >temp2
tr "[2*]" "[002*]" <temp2 >temp1
tr "[3*]" "[043*]" <temp1 >temp2
tr "[4*]" "[004*]" <temp2 >temp1
tr "[5*]" "[045*]" <temp1 >temp2
tr "[6*]" "[046*]" <temp2 >temp1
tr "[7*]" "[007*]" <temp1 >temp2
tr "[8*]" "[010*]" <temp2 >temp1
tr "[9*]" "[051*]" <temp1 >temp2
tr "[a*]" "[052*]" <temp2 >temp1
tr "[b*]" "[013*]" <temp1 >temp2
tr "[c*]" "[054*]" <temp2 >temp1
tr "[d*]" "[015*]" <temp1 >temp2
tr "[e*]" "[016*]" <temp2 >temp1
tr "[f*]" "[057*]" <temp1 >$2
rm temp1 temp2

```


APPENDIX F
ATAC PROGRAM

The following programs are listings of the Main System and Receiver Control programs for the ATAC. The assembly language is to the right of the absolute listing of the first three columns.

TIME: 15:22:49 03/21/77

PAGE

ATAC

LOC	OBJECT CODE	CARD IMAGE	CARDNUM
0117	A446	IOR R,EU,EL	55
0118	B106 776A	CHP I,EU,0776A	56
011A	C102 012A	BRCL EQ,EX2	57
011C	0000	NOP	58
011D	0000	NOP	59
011E	0000	NOP	60
011F	0000	NOP	61
			62
			63
			64
			65
0120	BCF0 0136	LDRM D,0,EXECS,16	66
0122	ED00 0230	BAL I,0,OUTPUT	67
0124	E101 014A	LDR I,1,EXCRLF	68
0126	ED00 0230	BAL I,0,OUTPU	69
0128	C107 0100	BRC I,7,EXEC	70
			71
			72
			73
012A	ED00 0500	BAL I,RET,WJ	74
012C	C107 0100	BRCL U,EXEC	75
			76
			77
			78
			79
012E	0000	NOP	80
012F	0000	NOP	81
0130	0000	NOP	82
0131	0000	NOP	83
0132	0000	NOP	84
0133	0000	NOP	85
0134	C107 0100	BRCL U,EXEC	86
			87
			88
			89
			90
			91
			92
			93
			94
0136		EXECS DS 20	95
014A	0001	EXCRLF DC 1	96
014B	000A	DC 00D0A	97
014C	0000	DC 0	98
014D	0003	DC 3	99
014E	4558	DC 04558	100
014F	4543	DC 04543	101
0150	0000	DC 0	102
			103
			104
			105
			106
			107

COMBINE FIRST TWO BYTES OF COMMAND

SEE IF REQUEST FOR WJ

GO CALL WJ

PATCH AREA FOR ANOTHER REQUEST

RESTORE REGISTERS

ECHO INPUT BUFFER

GET ADDRESS OF CR/LF BUFFER

OUTPUT CR/LF

GO TRY AGAIN

GO TO WJ

SAVE AREA FOR REGISTERS

CR/LF

COUNT

EX

EC

NULL

03/21/77

TIME: 15:22:49

ATAC

LOC	OBJECT CODE	CARD	IMAGE	CARDNUM
0151	9C00 01D6	KV2	EQU 12	161
0153	E101 0228	KV3	EQU 13	162
0155	ED00 0230	KDATA	EQU 14	163
0157	E10A FFBF	.	.	164
0159	E109 BFFF	.	.	165
015B	4015	.	.	166
015C	4016	.	.	167
015D	E101 01D7	.	.	168
015F	E107 8000	.	.	169
0161	D997	.	.	170
		.	.	171
		.	.	172
		.	.	173
		.	.	174
		.	.	175
		.	.	176
		.	.	177
		.	.	178
		.	.	179
		.	.	180
		.	.	181
		.	.	182
		.	.	183
		.	.	184
		.	.	185
		.	.	186
		.	.	187
		.	.	188
		.	.	189
		.	.	190
		.	.	191
		.	.	192
		.	.	193
		.	.	194
		.	.	195
		.	.	196
		.	.	197
		.	.	198
		.	.	199
		.	.	200
		.	.	201
		.	.	202
		.	.	203
		.	.	204
		.	.	205
		.	.	206
		.	.	207
		.	.	208
		.	.	209
		.	.	210
		.	.	211
		.	.	212
		.	.	213

VARIABLE 2
 VARIABLE 3
 INPUT DATA FROM KEYBOARD

SAVE RETURN ADDRESS
 GET ADDRESS OF BUFFER TO OUTPUT
 OUTPUT INITIAL BUFFER
 DEVICE ADDRESS FOR INPUT
 DEVICE ADDRESS FOR OUTPUT
 POSITION COUNTER = 1
 MAX POSITION USED = 1
 ADDRESS OF BUFFER TO REGISTER
 RESET CODE
 RESET KEYBOARD

 SET KEYBOARD ENTRY BUFFER TO ALL SPACES

SET COUNTER TO BUFFER LENGTH
 GET BUFFER ADDRESS
 CODE FOR SPACE
 STORE BLANK CODE
 DECREMENT COUNTER
 DO AGAIN IF COUNTER GT 0

RESET CODE
 RESET KEYBOARD

GET DATA
 DATA PRESENT ?
 NO DATA, WAIT

RESET CODE
 RESET KEYBOARD
 GET STATUS
 DATA STILL PRESENT ?
 KEEP TRYING TO CLEAR

 DATA OBTAINED

03/21/77

TIME: 15:22:49

ATAC

LOC	OBJECT CODE	CARD IMAGE	PAGE	CARDNUM
0179	A10E 007F	AND		214
017B	208E	IS,KDATA,0007F		215
017C	C105 0184	IS,KDATA,008		216
017E	6FF5	NE,KMR6		217
017F	C105 0169	ADD		218
0181	4015	IS,KDEC-1		219
0182	C107 0169	BRCL		220
		NZ,KMR3		221
		LDR		222
		IS,KPC,1		223
		U,KMR3		224
		BRCL		225
KMR6		CMP		226
0184	21CE	IS,KDATA,01C		227
0185	C105 0190	NE,KMR8		228
0187	6015	ADD		229
0188	B105 0050	IS,KPC,1		230
018A	C106 0169	CMP		231
018C	E105 0050	LE,KMR3		232
018E	C107 01B9	LDR		233
		U,KMR11		234
		BRCL		235
KMR8		CMP		236
0190	20DE	IS,KDATA,00D		237
0191	C102 01B9	EQ,KMR11		238
		BRCL		239
0193	22EE	IS,KDATA,02E		240
0194	C102 01B1	EQ,KMR10		241
		BRCL		242
0196	220E	IS,KDATA,020		243
0197	C102 01B1	EQ,KMR10		244
		BRCL		245
0199	230E	IS,KDATA,030		246
019A	C104 01AB	LT,KMR9		247
		BRCL		248
019C	239E	IS,KDATA,039		249
019D	C106 01B1	LE,KMR10		250
		BRCL		251
019F	241E	IS,KDATA,041		252
01A0	C104 01AB	LT,KMR9		253
		BRCL		254
01A2	25AE	IS,KDATA,05A		255
01A3	C106 01B1	LE,KMR10		256
		BRCL		257
01A5	261E	IS,KDATA,061		258
01A6	C104 01AB	LT,KMR9		259
		BRCL		260
01A8	27AE	IS,KDATA,07A		261
01A9	C106 01B1	LE,KMR10		262
		BRCL		263
		*****		264
		ILLEGAL ENTRY		265
		*****		266
KMR9		LDR		
	E101 022C	I,KBUF,KBILL		
01AB	ED00 0230	I,KRET,OUTPUT		
01AD	C107 0153	U,KMR1		
01AF		BRCL		
		GET ADDRESS OF ILLEGAL BUFFER		
		OUTPUT BUFFER		
		START OVER		

LOC	OBJECT CODE	CARD IMAGE	CARDNUM
01D7	0050	KEYBOARD ENTRY BUFFER	320
01D8		*****	321
		KBUFFER DC 80	322
		DS 80	323
		COUNT	324
		RESERVE	325
		*****	326
		START SYMBOL BUFFER	327
		*****	328
		*****	329
0228	0003	KBSTRT DC 3	330
0229	000A	DC 000A	331
022A	002B	DC 002B	332
022B	0000	DC 0000	333
		COUNT	334
		CR/LF	335
		+	336
		NULL	337
		*****	338
		ILLEGAL CHARACTER BUFFER	339
		*****	340
		*****	341
022C	0003	KBELL DC 3	342
022D	0A07	DC 0A07	343
022E	0707	DC 0707	344
022F	0000	DC 0000	345
		COUNT	346
		CR, BELL	347
		BELL, BELL	348
		NULL	349
		*****	350
		OUTPUT	351
		ROUTINE TO OUTPUT TO THE TTY/CRT	352
		*****	353
		CALLING PROCEDURE:	354
		BAL 1,0,OUTPUT	355
		*****	356
		INPUTS:	357
		REG 1 ADDRESS OF BUFFER TO BE OUTPUT	358
		*****	359
		THE BUFFER MUST BE SET UP IN THE FOLLOWING MANNER:	360
		WORD 1 N = NUMBER OF WORDS IN BUFFER TO BE OUTPUT	361
		WORDS 2-N ASCII DATA TO BE OUTPUT, TWO ASCII	362
		CHARACTERS PER WORD	363
		*****	364
		OUTPUTS:	365
		NONE	366
		ROUTINES CALLED:	367
		NONE	368
		*****	369
		THIS ROUTINE PRESERVES NO REGISTERS	370
		*****	371
		*****	372

03/21/77

TIME: 15:22:49

ATAC

LOC

OBJECT CODE

CARD IMAGE

CARDNUM

PAGE

 : ESTABLISH EQUATES
 : *****

BUFAD EQU 1
 BO EQU 5
 VIN EQU 6
 VOUT EQU 7
 VL EQU 8
 VU EQU 9
 WO EQU 10
 WI EQU 11
 VIU EQU 12
 VIL EQU 13
 STAT EQU 14
 WOUT EQU 15

ADDRESS OF BUFFER TO OUTPUT
 OUTPUT BUFFER ADDRESS
 INPUT DEVICE ADDRESS
 OUTPUT DEVICE ADDRESS
 INPUT BUFFER LOWER BYTE
 INPUT BUFFER UPPER BYTE
 NUMBER OF WORDS TO OUTPUT
 UPPER BYTE INDEX
 LOWER BYTE INDEX
 STATUS
 WORD TO OUTPUT TO TTY

 : INITIALIZE AND SET UP CONSTANTS
 : *****

OUTPUT LDR IS,VIU,0
 LDR IS,VIL,0FFBF
 LDR I,VIN,0BFFF
 LDR I,VOUT,0BFFF
 LDR RX,WI,VIU,BUFAD
 STR D,VIU,COUNT
 CMP IS,WI,0
 BRCL LE,OUT4
 CMP IS,WI,40
 BRCL LE,OUT3
 STR D,WI,COUNT
 LDR IS,WI,40
 LDR RX,WI,VIU,0
 SHS LL,WI,0
 LDR I,BO,BUFOUT

INDEX FOR STORING UPPER BYTE
 INDEX FOR STORING LOWER BYTE
 INPUT DEVICE ADDRESS
 OUTPUT DEVICE ADDRESS
 GET INPUT WORD COUNT
 INITIALIZE COUNT
 COMPARE WORD COUNT WITH ZERO
 GET OUT IF COUNT LESS THAN ZERO
 COMPARE WITH MAX VALUE
 IF IN LIMIT KEEP GOING
 SAVE ORIGINAL COUNT
 ONLY OUTPUT 40 WORDS
 PUT IN OUTPUT WORD COUNT
 DOUBLE FOR OUTPUT WORD COUNT
 GET OUTPUT BUFFER ADDRESS

 : TRANSFER INPUT BYTE BUFFER TO OUTPUT WORD BUFFER
 : *****

OUT1 ADD IS,BUFAD,1
 LDR RX,VU,VIU,BUFAD
 LDR RX,VL,VIU,0
 SHS RL,VL,8
 SHS RL,VL,8
 SHS RL,VU,8
 STR RX,VU,VIU,BO
 STR RX,VL,VIL,BO

INCREMENT INPUT POINTER TO NEXT ENTR
 GET INPUT WORD IN UPPER BYTE REGISTE
 PUT IN LOWER BYTE REGISTER ALSO
 CLEAR UPPER BYTE
 RIGHT JUSTIFY LOWER BYTE
 RIGHT JUSTIFY UPPER BYTE
 STORE UPPER BYTE AS FULL WORD
 IN THE OUTPUT BUFFER
 STORE LOWER BYTE AS FULL WORD

03/21/77

TIME: 15:22:49

PAGE

ATAC

LOC	OBJECT CODE	CARD IMAGE	CARDNUM
024E	6025	ADD IS,BO,2	426
024F	6FFB	ADD IS,RI,-1	427
0250	C101 0246	BRCL GT,OUT1	428
		IN THE OUTPUT BUFFER	429
		INCREMENT OUTPUT BUFFER POINTER	430
		DECREMENT NUMBER OF WORDS TO INPUT	431
		DO AGAIN IF NOT FINISHED	432
		*****	433
		OUTPUT WORD BUFFER	434
		*****	435
0252	F105 026B	LDR I,BO,BUPOUT	436
0254	8C6E 1000	RIN SP,WIN	437
0255	9E0E 1000	IF,STAT,01000	438
0257	C105 0254	BRCL NE,OUT2	439
0259	B75F 0000	LLC DX,OUT2	440
025B	A10F 01FF	AND I,OUT,00FF	441
025D	D97F	ROUT WOUT,VOUT	442
025E	6015	ADD IS,BO,1	443
025F	6FFA	ADD IS,BO,-1	444
0260	C101 0254	BRCL GT,OUT2	445
		GET ADDRESS OF OUTPUT BUFFER	446
		GET STATUS	447
		COMPARE STATUS	448
		WAIT IF NOT READY	449
		GET CHARACTER TO OUTPUT	450
		CLEAR ALL BUT OUTPUT DATA	451
		OUTPUT A CHARACTER	452
		INCREMENT BUFFER POINTER	453
		DECREMENT WORD COUNTER	454
		GO OUTPUT ANOTHER CHARACTER	455
		*****	456
		EXIT	457
		*****	458
0262	F20B 026A	LDR D,WI,COUNT	459
0264	C102 0269	BRCL Z,OUT4	460
0266	6D8B	ADD IS,WI,-40	461
0267	C107 0237	BRCL U,OUT5	462
0269	BF07	BRC R,7,RET	463
		GET EXCESS COUNT	464
		GET OUT IF ZERO	465
		DECREMENT BY 40	466
		DO AGAIN	467
		*****	468
026A		COUNT DS 1	469
026B		BUFOUT DS 80	470
		SAVE LOCATION FOR EXCESS COUNT	471
		OUTPUT BUFFER	472
		*****	473
		HEX	474
		ROUTINE TO CONVERT HEX TO ASCII	475
		CALLING PROCEDURE:	476
		DAL I,0,HEXA	477
		INPUTS:	478
		REG 1 HEX VALUE TO BE CONVERTED (INTEGER)	
		OUTPUTS:	

CARDNUM

CARD IMAGE

OBJECT CODE

LOC

```

. . . REG 2 MOST SIGNIFICANT TWO DIGITS IN ASCII *
. . . REG 3 LEAST SIGNIFICANT TWO DIGITS IN ASCII *
. . . LETTERS ARE OUTPUT IN UPPER CASE *
. . . ROUTINES CALLED: *
. . . NONE *
. . . THIS ROUTINE DOES NOT DISTURB REGISTERS 5 THROUGH 15 *
. . . *****
. . . ESTABLISH EQUATES *****
. . . *****
HIN EQU 1
MSD EQU 2
LSD EQU 3
V1 EQU 4
. . .
. . . *****
. . . CONVERT TO ASCII *****
. . . *****
HEXA STR D,RET,HEXRTN
E014 LDR R,V1,HIN
ADB4 SHS R,V1,12
E000 BAL I,RET,HEXA1
AE74 SHS LL,V1,8
E042 LDR R,MSD,V1
E014 LDR R,V1,HIN
AD74 SHS R,V1,8
A104 AND I,V1,0000F
E000 BAL I,RET,HEXA1
E042 ADD R,MSD,V1
E014 LDR R,V1,HIN
A104 AND I,V1,0000F
E034 SHS RL,V1,4
E000 BAL I,RET,HEXA1
AE74 SHS LL,V1,8
E043 LDR R,LSD,V1
E014 LDR R,V1,HIN
A104 AND I,V1,OF
E000 BAL I,RET,HEXA1
E043 ADD R,LSD,V1
. . .
. . . *****
. . . EXIT *****
. . .

```

HEX VALUE INPUT
MOST SIGNIFICANT DIGITS TO OUTPUT
LEAST SIGNIFICANT DIGITS TO OUTPUT
VARIABLE

SAVE RETURN REGISTER
GET HEX INPUT VALUE
RIGHT JUSTIFY FIRST DIGIT
CONVERT FIRST DIGIT
POSITION DIGIT REGISTER
PUT IN OUTPUT VALUE
GET HEX INPUT VALUE
RIGHT JUSTIFY SECOND DIGIT
CLEAR ALL BUT SECOND DIGIT
CONVERT SECOND DIGIT
PUT IN OUTPUT REGISTER
GET HEX INPUT VALUE
CLEAR ALL BUT THIRD DIGIT
RIGHT JUSTIFY THIRD DIGIT
CONVERT THIRD DIGIT
POSITION DIGIT REGISTER
PUT IN OUTPUT REGISTER
GET HEX INPUT VALUE
CLEAR ALL BUT FOURTH DIGIT
CONVERT FOURTH DIGIT
PUT IN OUTPUT REGISTER

03/21/77

TIME: 15:22:49

PAGE

ATAC

CARDNUM

CARD IMAGE

OBJECT CODE

LOC

02D8 E200 02E1 LDR D,RET,HEXRTN GET RETURN ADDRESS
02DA BF07 BRC R,7,RET RETURN

* CONVERT ONE DIGIT
* *****

02DB 20A4 CMP IS,V1,00A COMPARE WITH HEX 'A'
02DC C104 BRCL LI,HEXA2 BRANCH IF LESS
02DE 6074 ADD IS,V1,7 ADD 7 TO VALUE
02DF 6304 ADD IS,V1,030 ADD HEX '30'
02E0 BF07 BRC R,7,RET GO BACK TO WHERE CALLED FROM

* DATA
* ***

02E1 HEXRTN DS 1 SAVE LOCATION FOR RETURN ADDRESS

* AHEX

ROUTINE TO CONVERT FOUR (4) OR LESS DIGITS IN ASCII
CODE TO A TRUE HEX VALUE FOR THE MACHINE. SIGN OF THE
VALUE MUST BE HANDLED BY THE CALLING ROUTINE.

CALLING PROCEDURE:
BAL I,0,AHEX

INPUTS:
REG 1 ADDRESS OF FIRST CONSECUTIVE LOCATION IN
CORE WHERE THE ASCII CHARACTERS ARE LOCATED
(ONE CHARACTER PER CORE LOCATION)

OUTPUT:
REG 2 HEX VALUE

ROUTINES CALLED:
NONE

REGISTERS 8 THROUGH 16 ARE PRESERVED

* ESTABLISH EQUATES
* *****

AHADD EQU 1 ADDRESS OF ASCII CHARACTERS
AHOUT EQU 2 OUTPUT HEX VALUE
AHV1 EQU 5 VARIABLE 1

ATAC

LOC	OBJECT CODE	CARD IMAGE	CARDNUM
		CV3 EQU 5	VARIABLE 3
		CHAX EQU 6	MAX NO. CHARACTERS INEUT BY KFYMR
		CINDX EQU 7	PATH FLAG
		CFLG EQU 8	BLANK FLAG
		CF2 EQU 9	FIELD2
		CZERO EQU 10	CONSTANT 0 FOR SPACE
		CSPACE EQU 11	ASCII CODE
		CV1 EQU 12	VARIABLE 1
		CV2 EQU 13	VARIABLE 2
		CMD EQU 14	COMMAND
		CP1 EQU 15	FIELD 1
		.	
		.	
		.	
		. ****	
		. SET UP	
		. *****	
		.	
		. CORE	SAVE REGISTER 2
02F8	9C02 03D3	STR D,2,CSAVE	GET A ZERO
02FA	400C	IS, CV1, 0	INITIALIZE SEQUENTIAL CHANGE FLAG
02FB	9C0C	LDR D, CV1, CSPLG	GET BUFFER ADDRESS FOR TITLE
02FD	E101 0405	I, CADD, 0	OUTPUT TITLE
02FF	E000 0230	I, RET, OUTPUT	GET KEYBOARD COMMAND
0301	E000 0151	I, RET, KEYHR	SET UP SPACE CODE
0303	E10B 2020	IS, CSPACE, 02020	SET UP ZERO CONSTANT
0305	400A	IS, CZERO, 0	ZERO COMMAND REGISTER
0306	400E	IS, CMD, 0	ZERO FIELD 1
0307	400F	IS, CF1, 0	ZERO FIELD 2
0308	4009	IS, CF2, 0	ZERO FLAG
0309	4008	IS, CFLG, 0	ZERO PATH FLAG
030A	4007	LDR IS, CINDX, 0	
		.	
		. *****	
		. TRANSLATE COMMAND	
		. *****	
		.	
		. C2	GET NO. OF ENTRIES IN BUFFER
		. C3	SET FLAG FOR READY
030B	51A6	LDR RX, CHAX, CZERO, CADD	INCREMENT BUFFER ADDRESS
030C	4008	LDR IS, CFLG, 0	DECREMENT CHARACTER COUNTER
030D	6011	ADD IS, CADD, 1	DONE
030E	6FF6	BRCL NP, C6A	GET A CHARACTER FROM THE BUFFER
030F	C106 0327	LDR RX, CV1, CZERO, CADD	COMPARE WITH SPACE
0311	51AC	CHP IS, CV1, 020	KEEP GOING IF SPACE
0312	220C	BRCL EQ, C2	SEE IF IN MIDDLE OF ENTRY
0313	C102 030C	CMP IS, CFLG, 0	IN ENTRY, KEEP LOOKING
0315	2008	BRCL NE, C3	
0316	C105 030D		
		.	
0318	E370 031B	LDR DX, RET, CFLD, CINDX	GET PROCESSING ADDRESS
031A	BF07	BRC R, 7, RET	PROCESS ACCORDING TO FIELD FOUND
		.	
		. BRANCH TABLE	
		.	

03/21/77

TIME: 15:22:49

ATAC

CARDNUM

CARD IMAGE

OBJECT CODE

CFLD

C4

C5

C6

C7

C8

C9

C10

C11

C12

C13

C14

C15

C16

C17

C18

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C358

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C360

C361

C362

CARDNUM

CARD IMAGE

OBJECT CODE

LOC

034A	C102 039C	.	BRCL EQ,C12	GO PROCESS 'CHANGE'	797
034C	B10C 6373	.	CMP I,CV1,06373	COMPARE WITH 'CS'	798
034E	C102 03A0	.	BRCL EQ,C20	GO PROCESS CHANGE SEQUENTIAL	799
0350	C107 02FD	.	BRCL U,C1	INVALID COMMAND, GO TRY AGAIN	800
		.			801
		.			802
		.			803
		.			804
		.			805
		.			806
		.			807
		.			808
		.			809
		.			810
0352	E200 03D3	C9	LDR D,0,CSAVE	GET ADDRESS OF CALLING ROUTINE	811
0354	C107 0151	.	BRC I,7,KEYMR	EXIT THROUGH KEYMR	812
		.			813
		.			814
		.			815
		.			816
		.			817
		.			818
		.			819
		.			820
0356	A10F FFF8	C10	AND I,CF1,OFFP8	CLEAR LAST THREE BITS	821
0358	E0F5	.	LDR R,CV3,CF1	SET UP ADDRESS TO DUMP	822
0359	40A7	.	LDR IS,CINDX,10	SET UP LINE COUNTER	823
		.			824
		.			825
		.			826
035A	E10C 03D5	C13	LDR I,CV1,CBUFF	SET UP OUTPUT BUFFER ADDRESS	827
035C	E0AD	.	LDR R,CV2,CZERO	SET UP ROW COUNTER	828
035D	E051	.	LDR R,CADD,CV3	SET UP INPUT FOR HEXA	829
035E	E000	.	BAL I,RET,HEXA	CONVERT ADDRESS TO ASCII	830
0360	1AC2	.	STR RX,CA1,CV1,CZERO	PUT MSD OF ADD IN OUTPUT BUFFER	831
0361	601C	.	ADD IS,CV1,1	INCREMENT BUFFER ADDRESS	832
0362	1AC3	.	STR RX,CA2,CV1,CZERO	PUT LSD OF ADD IN OUTPUT BUFFER	833
0363	601C	.	ADD IS,CV1,1	INCREMENT BUFFER ADDRESS	834
0364	1ACB	.	STR RX,CSPACE,CV1,CZERO	PUT IN SPACES	835
0365	601C	.	ADD IS,CV1,1	INCREMENT BUFFER ADDRESS	836
0366	1ACB	.	STR RX,CSPACE,CV1,CZERO	PUT IN SPACES	837
0367	5A11	.	ADD IS,CV1,1	INCREMENT BUFFER ADDRESS	838
0368	5A51	.	LDR RX,CADD,CV3,CZERO	GET VALUE TO CONVERT	839
0369	6015	.	ADD IS,CV3,1	INCREMENT ADD OF VALUE TO OUTPUT	840
036A	E000	.	BAL I,RET,HEXA	CONVERT VALUE	841
036C	1AC2	.	STR RX,CA1,CV1,CZERO	PUT MSD OF VALUE IN OUTPUT BUFFER	842
036D	601C	.	ADD IS,CV1,1	INCREMENT BUFFER ADDRESS	843
036E	1AC3	.	STR RX,CA2,CV1,CZERO	PUT LSD OF VALUE IN OUTPUT BUFFER	844
036F	601D	.	ADD IS,CV2,1	INCREMENT ROW COUNTER	845
0370	208D	.	CHP IS,CV2,8	COMPARE WITH LAST VALUE	846
0371	0375	.	EQ C15	BRANCH IF EQUAL	847
0373	C107 0365	.	BRCL U,C14	GO DO ANOTHER VALUE	848
0375	E101 03D5	C15	LDR I,CADD,CBUFF	GET BUFFER POINTER	849

LOC	OBJECT CODE	CARD IMAGE	CARDNUM
0377	6FF1	ADD	850
0378	9CF0	STRM	851
0379	ED00	BAL	852
037C	BCF0	LDRM	853
037E	6FF7	ADD	854
037F	C105	BRC	855
0381	C107	BRC	856
.	.	.	857
.	.	.	858
.	.	.	859
.	.	.	860
.	.	.	861
.	.	.	862
.	.	.	863
.	.	.	864
C11	E0F1	LDR	865
0383	ED00	BAL	866
0384	9C02	STR	867
0386	9C03	STR	868
0388	E3F1	LDR	869
038A	E101	BAL	870
038C	ED00	STR	871
038E	9C02	STR	872
0390	9C03	STR	873
0392	E101	LDR	874
0394	ED00	BAL	875
0396	E20F	LDR	876
0398	C105	BRC	877
039A	C107	BRC	878
.	.	.	879
.	.	.	880
.	.	.	881
.	.	.	882
.	.	.	883
.	.	.	884
C12	9BF9	STR	885
039C	C107	BRC	886
039E	C107	BRC	887
.	.	.	888
.	.	.	889
.	.	.	890
.	.	.	891

CARDNUM

CARD IMAGE

OBJECT CODE

03A0	9C0F	0410	STR	D,CF1,CSTRT	SAVE START OF CORE CHANGE	892
03A2	9C0F	0411	STR	D,CF1,CSTOR	SAVE ADDRESS AT WHICH TO STORE	893
03A4	401C		LDR	IS,CV1,1	SET UP A CONSTANT 1	894
03A5	9C0C	0412	STR	D,CV1,CSFLG	SET FLAG FOR SEQUENTIAL CHANGE	895
03A7	ED00	0151	BAL	I,GET,KEYMR	GET VALUE FOR CORE	896
03A9	400A		LDR	IS,CZERO,0	SET UP ZERO REGISTER	897
03AA	6011		ADD	IS,CADD,1	INCREMENT BUFFER POINTER	898
03AB	4015		LDR	IS,CV3,1	SET UP A CONSTANT 1	899
03AC	51AC		LDR	RX,CV1,CZERO,CADD	GET FIRST CHARACTER ENTERED	900
03AD	515D		LDR	RX,CV2,CV3,CADD	GET SECOND CHARACTER ENTERED	901
03AE	AE7C		SHS	LL,CV1,8	LEFT JUSTIFY FIRST CHARACTER	902
03AF	AE7D		SHS	LL,CV2,8	CLEAR UPPER 8 BITS OF SECOND CHAR	903
03B0	AD7D		SHS	RL,CV2,8	RIGHT JUSTIFY SECOND CHARACTER	904
03B1	80DC		ADD	R,CV1,CV2	COMBINE BOTH CHARACTERS	905
03B2	B10C		CMP	I,CV1,0646P	COMPARE WITH 'DO'	906
03B4	C102	646F	BRCL	E,C22,1	GET OUT IF DONE	907
03B6	E200	02E2	BAL	I,GET,AHXX	CONVERT ENTRY TO HEX	908
03B8	E20F	0411	LDR	D,CF1,CSTOR	GET ADDRESS FOR STORING	909
03BA	9BF2	0000	STR	DX,CA1,0,CF1	PUT VALUE IN CORE	910
03BC	601F		ADD	IS,CF1,1	INCREMENT STORE ADDRESS	911
03BD	9C0F	0411	STR	D,CF1,CSTOR	SAVE NEW STORE ADDRESS	912
03BF	C107	03A7	BRCL	U,C21,1	GO GET ANOTHER ENTRY	913
03C1	E20F	0410	LDR	D,CF1,CSTRT	GET ADDRESS OF FIRST CORE CHANGED	914
03C3	C107	03B3	BRCL	U,C11,1	GO DISPLAY LOCATION	915
03C5	E20C	0410	LDR	D,CV1,CSTRT	GET ADDRESS DISPLAYED	916
03C7	601C		ADD	IS,CV1,1	INCREMENT ADDRESS	917
03C8	9C0C	0410	STR	D,CV1,CSTRT	SAVE AS NEW DISPLAY ADDRESS	918
03CA	B20A	0411	CMP	D,CV1,CSTOR	COMPARE WITH LAST ADDRESS+1	919
03CC	C104	03C1	BRCL	LT,C22,1	DO AGAIN IF NOT FINISHED	920
03CE	400C		LDR	IS,CV1,0	GET A ZERO SEQUENTIAL FLAG	921
03CF	9C0C	0412	STR	D,CV1,CSFLG	CLEAR SEQUENTIAL FLAG	922
03D1	C107	02FD	BRCL	U,C1,1	GO GET ANOTHER COMMAND	923
03D3						924
03D4	001C					925
03D5	000A					926
03F0	0D0A					927
						928
						929
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						943
						944

ADDRESS OF ROUTINE CALLING CORE

COUNT OF VALUES IN BUFFER TO OUTPUT
OUTPUT BUFFER
CR/LF

DATA AND BUFFERS

CSAVE DS 1

CBICNT DC 28
CBUFF DS 27
DC 00D0A

03/21/77

TIME: 15:22:49

ATAC

LOC	OBJECT CODE	CARD IMAGE	REG SAVE AREA FOR INTERNAL USE	CARDNUM
03F1		CS1 DS 20		945
0405	0003	CTITLE		946
0406	0D0A	DC	COUNT	947
0407	434F	DC	CR/LF	948
0408	5245	DC	CO	949
			RE	950
0409	0006	CBUD	COUNT	951
040A		CBUD1 DS 2	2 LOCATIONS FOR ADDRESS	952
040C	2020	DC	BLANKS	953
040D		DS 2	2 LOCATIONS FOR CONTENTS	954
040F	0D0A	DC	CR/LF	955
0410	0000	CSTRT	START ADDRESS FOR SEQUENTIAL CORE	956
0411	0000	CSTOR	CURRENT ADDRESS FOR STORING IN SEQ	961
0412	0000	CSFLG	FLAG FOR SEQUENTIAL CHANGE	962
				963
				964
				965
				966

LOC	OBJECT CODE	CARD IMAGE	CARDNUM
0000		IDT ATAC DS 0500 ENTRY WJ RET EQU 0 OUTPUT EQU 00230 KEYMR EQU 00151 . . ***** . ESTABLISH EQUATES . ***** WJXS EQU 1 WJXE EQU 2 WJX1 EQU 3 WJX2 EQU 4 WJX3 EQU 5 WJX4 EQU 6 WJD1 EQU 7 WJD2 EQU 8 WJD3 EQU 9 WJD4 EQU 10 WJXX EQU 11 WJV1 EQU 1 WJV2 EQU 2 WJV3 EQU 3 WJV4 EQU 4 WJV5 EQU 5 WJV6 EQU 6 WJV7 EQU 7 WJV8 EQU 8 WJV9 EQU 9 WJV10 EQU 10 WJV11 EQU 11 WJLPC EQU 15 . . . ***** . ENTRY . ***** WJ . . ***** . INITIALIZE RECEIVER . ***** WJ01 LDRM D,WJV1,WJ11,4 BC31 09BC STRM D,WJV1,WJCW1,4 0504 9C31 09C8 STRM D,WJV1,WJICD,8 0506 BC71 09C0 LDRM D,WJV1,WJCFL,8 0508 9C71 09D8 STRM D,WJV1,WJCFL,8	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54
0500	9C00 09AD	WJ . . ***** . SAVE RETURN ADDRESS . ***** WJ . . ***** . INITIALIZE RECEIVER . ***** WJ01 LDRM D,WJV1,WJ11,4 BC31 09BC STRM D,WJV1,WJCW1,4 0504 9C31 09C8 STRM D,WJV1,WJICD,8 0506 BC71 09C0 LDRM D,WJV1,WJCFL,8 0508 9C71 09D8 STRM D,WJV1,WJCFL,8	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54
0502	BC31 09BC	WJ01 LDRM D,WJV1,WJ11,4 BC31 09BC STRM D,WJV1,WJCW1,4 0504 9C31 09C8 STRM D,WJV1,WJICD,8 0506 BC71 09C0 LDRM D,WJV1,WJCFL,8 0508 9C71 09D8 STRM D,WJV1,WJCFL,8	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54

XAR START
 XAR END
 XAR 1
 XAR 2
 XAR 3
 XAR 4
 DATA 1
 DATA 2
 DATA 3
 DATA 4
 XAR FOR CHECK
 VARIABLE 1
 VARIABLE 2
 VARIABLE 3
 VARIABLE 4
 VARIABLE 5
 VARIABLE 6
 VARIABLE 7
 VARIABLE 8
 VARIABLE 9
 VARIABLE 10
 VARIABLE 11
 WJS COUNTER

ATAC

LOC	OBJECT CODE	CARD	IMAGE	CARDNUM
0539	C107 0531	BRCL	U, WJ10	108
053B	9C03 09D0	STR	D, WJ3, WJTFL	109
053D	9C04 09D1	STR	D, WJ4, WJTFF	110
			ILLEGAL FREQUENCY	111
			STORE TENTATIVE FREQUENCY {LOWER}	112
			STORE TENTATIVE FREQUENCY {UPPER}	113
053F	E101 0A89	LDR	I, WJ1, WJDMB	114
0541	E000 07AE	BAL	I, RET, WJ90	115
0543	C107 053F	BRCL	U, WJ11	116
0545	2073	CHP	IS, WJ3, 7	117
0546	C101 053P	BRCL	GT, WJ11	118
0548	9C03 09D2	STR	D, WJ3, WJTDH	119
054A	E101 0004	LDR	I, WJ1, 04	120
054C	5C01 09D4	STR	D, WJ1, WJTBU	121
054E	E101 5500	LDR	I, WJ1, 05500	122
0550	9C01 09D3	STR	D, WJ1, WJTBL	123
0552	2033	CHP	IS, WJ3, 3	124
0553	C105 056E	BRCL	NE, WJ13	125
			NOT VARIABLE BFO, USE DEFAULT FREQUE	126
			OUTPUT TITLE AND GET KEYBOARD ENTRY FOR BFO FREQUENCY	127
0555	E101 0AB3	LDR	I, WJ1, WJBFB	128
0557	E000 07AE	BAL	I, RET, WJ90	129
0559	C107 0555	BRCL	U, WJ12	130
055B	2062 0555	CHP	IS, WJ2, 6	131
055C	C105 0555	BRCL	NE, WJ2	132
055E	E833	SHD	RL, WJ3, 4	133
055F	2044	CHP	IS, WJ4, 04	134
0560	C105 0555	BRCL	NE, WJ12	135
0562	B103 4500	CHP	I, WJ3, 04500	136
0564	C104 0555	BRCL	LF, WJ12	137
0566	B103 6500	CHP	I, WJ3, 06500	138
0568	C101 0555	BRCL	GF, WJ12	139
056A	9C03 09D3	STR	D, WJ3, WJTBL	140
056C	9C04 09D4	STR	D, WJ4, WJTBU	141
			SAVE TENTATIVE BFO FREQUENCY {LOWER}	142
			SAVE TENTATIVE BFO FREQUENCY {UPPER}	143
			OUTPUT TITLE AND GET KEYBOARD ENTRY FOR GAIN MODE	144
056E	E101 0A53	LDR	I, WJ1, WJGMB	145
0570	E000 07AE	BAL	I, RET, WJ90	146
0572	C107 056E	BRCL	U, WJ13	147
0574	2033	CHP	IS, WJ3, 3	148
0575	C101 056E	BRCL	GT, WJ11	149
0577	2013	CHP	IS, WJ3, 1	150
0578	C102 056E	BRCL	EQ, WJ13	151
057A	E201 09D2	LDR	D, WJ1, WJTDH	152
057C	2041	CHP	IS, WJ1, 4	153
057D	C105 0582	BRCL	NE, WJ13	154
057F	2003	CHP	IS, WJ3, 0	155
0580	C102 056E	BRCL	EQ, WJ13	156
0582	9C03 09D5	STR	D, WJ3, WJTGM	157
			MAKE SURE GAIN MODE NOT HOLD AGC	158
			SAVE TENTATIVE GAIN MODE	159
			OUTPUT TITLE AND GET KEYBOARD ENTRY FOR IF BANDWIDTH	160

CARDNUM

ATAC

LOC OBJFCT CODE

CARD IMAGE

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0584 E201 09D2      .      LDR      D,WJV1,WJTDH      GET TENTATIVE DETECT MODE
0586 2041      CMP      IS,WJV1,4      COMPARE WITH IS
0587 C104 058F      BRCL     LT,WJV14      NOT SIDE BAND-BRANCH
0589 2061      CMP      IS,WJV1,6      COMPARE WITH USE
058A C101 058F      BRCL     GT,WJV14,6      NOT SIDE BAND-BRANCH
058C 4043      LDR      IS,WJV3,4      LOAD DEFAULT IF BANDWIDTH
058D C107 059B      BRCL     U,WJV14,1      SKIP IF BANDWIDTH
058E E001 0A6D      LDR      I,WJV1,WJIFB      GET ADDRESS OF IF BANDWIDTH TITLE
0591 ED00 07AE      BAL      I,RET,WJ90      OUTPUT TITLE AND GET ENTRY
0593 C107 058F      BRCL     U,WJV14      ILLEGAL ENTRY
0595 2043      CMP      IS,WJV3,4      COMPARE WITH MAX VALUE
0596 C101 058F      BRCL     GT,WJV14,1      ILLEGAL ENTRY
0598 2013      CMP      IS,WJV3,1      COMPARE WITH MIN VALUE
0599 C104 058F      BRCL     LT,WJV14      ILLEGAL ENTRY
059B 9C03 09D7      STR      D,WJV3,WJTIF      SAVE TENTATIVE IF BANDWIDTH

: OUTPUT TITLE AND GET KEYBOARD ENTRY FOR RF GAIN
WJ15  LDR      I,WJV1,WJRGB      GET ADDRESS OF RF GAIN TITLE
      UAL      I,RET,WJ90      OUTPUT TITLE AND GET ENTRY
      CMP      IS,WJV2,3      ILLEGAL ENTRY
      CMP      I,WJV3,0100      ILLEGAL ENTRY
      STR      D,WJV3,WJTRFG      ILLEGAL ENTRY
      BRCL     U,WJ02      SAVE TENTATIVE RF GAIN
      GO GET ANOTHER COMMAND

:
:
:
: ***** CONTROL WORD (COMMAND=1) *****
: ***** DISPLAY TENTATIVE *****
WJ20  LDR      D,WJV2,WJTFL      GET UPPER OF TENTATIVE FREQUENCY
      LDR      D,WJV1,WJTFL      GET LOWER OF TENTATIVE FREQUENCY
      BAL      I,RET,WJ92      PUT FREQUENCY IN BUFFER AND DISPLAY
      LDR      D,WJV1,WJTGH      GET TENTATIVE GAIN MODE
      LDR      D,WJV2,WJTIF      GET TENTATIVE IF BANDWIDTH
      BAL      I,RET,WJ93      OUTPUT GAIN MODE AND IF BANDWIDTH
      LDR      D,WJV1,WJTDH      GET TENTATIVE DETECT MODE
      LDR      D,WJV2,WJTBL      GET TENTATIVE BFO FREQUENCY (LOWER)
      BAL      I,RET,WJ94      OUTPUT DETECT MODE AND BFO FREQUENCY
      LDR      D,WJV1,WJTRFG      GET TENTATIVE RF GAIN
      BAL      I,RET,WJ95      OUTPUT RF GAIN
      BRCL     U,WJ02      DONE
      .
      .
      .
05AE E202 09D1      WJ20  LDR      D,WJV2,WJTFL      GET UPPER OF TENTATIVE FREQUENCY
05E0 E201 09D0      LDR      D,WJV1,WJTFL      GET LOWER OF TENTATIVE FREQUENCY
05E2 ED00 07D9      BAL      I,RET,WJ92      PUT FREQUENCY IN BUFFER AND DISPLAY
05E4 E201 09D5      LDR      D,WJV1,WJTGH      GET TENTATIVE GAIN MODE
05E6 E202 09D7      LDR      D,WJV2,WJTIF      GET TENTATIVE IF BANDWIDTH
05E8 ED00 0801      BAL      I,RET,WJ93      OUTPUT GAIN MODE AND IF BANDWIDTH
05EA E201 09D2      LDR      D,WJV1,WJTDH      GET TENTATIVE DETECT MODE
05EC E202 09D3      LDR      D,WJV2,WJTBL      GET TENTATIVE BFO FREQUENCY (LOWER)
05EE ED00 0820      BAL      I,RET,WJ94      OUTPUT DETECT MODE AND BFO FREQUENCY
05C0 E201 09D6      LDR      D,WJV1,WJTRFG      GET TENTATIVE RF GAIN
05C2 ED00 084A      BAL      I,RET,WJ95      OUTPUT RF GAIN
05C4 C107 0519      BRCL     U,WJ02      DONE
      .
      .
      .

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LOC	OBJECT CODE	CARD IMAGE	CARDNUM
05C6	E202 09D9	***** : DISPLAY CONTROL WORD (COMMAND=2) : *****	214
05C8	E201 09D8	*****	215
05CA	E200 07D9	*****	216
05CC	E201 09D0	*****	217
05CE	E202 09DF	*****	218
05CF	E200 0801	*****	219
05D2	E201 09DA	*****	220
05D4	E202 09DB	*****	221
05D6	E200 0820	*****	222
05D8	E201 09DE	*****	223
05DA	E200 084A	*****	224
05DC	C107 0519	*****	225
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		*****	238
05DE	E202 09E1	*****	239
05E0	E201 09E0	*****	240
05E2	E200 07D9	*****	241
05E4	E201 09E5	*****	242
05E6	E202 09E7	*****	243
05E8	E200 0801	*****	244
05EA	E201 09E2	*****	245
05EC	E202 09E3	*****	246
05EE	E200 0820	*****	247
05F0	E201 09E6	*****	248
05F2	E200 084A	*****	249
05F4	E201 09E9	*****	250
05F6	4002	*****	251
05F7	P871	*****	252
05F8	A502 2030	*****	253
05FA	9C02 0022	*****	254
05FC	4002	*****	255
05FD	F831	*****	256
05FE	A832	*****	257
05FF	F831	*****	258
0600	A502 3030	*****	259
0602	9C02 0023	*****	260
0604	E101 0018	*****	261
0606	E100 0230	*****	262
0608	C107 0519	*****	263
060A		*****	264
		*****	265
		*****	266

GET UPPER OF CONTROL FREQUENCY
GET LOWER OF CONTROL FREQUENCY
OUTPUT FREQUENCY
GET CONTROL GAIN MODE
GET CONTROL IF BANDWIDTH
OUTPUT GAIN MODE AND IF BANDWIDTH
GET CONTROL DETECT MODE
GET CONTROL BFO FREQUENCY (LOWER)
OUTPUT DETECT MODE AND BFO FREQUENCY
GET CONTROL RF GAIN
OUTPUT RF GAIN
DONE

GET UPPER OF RECEIVED FREQUENCY
GET LOWER OF RECEIVED FREQUENCY
OUTPUT FREQUENCY
GET RECEIVED GAIN MODE
GET RECEIVED IF BANDWIDTH
OUTPUT GAIN MODE AND IF BANDWIDTH
GET RECEIVED DETECT MODE
GET RECEIVED BFO FREQUENCY (LOWER)
OUTPUT DETECT MODE AND BFO FREQUENCY
GET RECEIVED RF GAIN
OUTPUT RF GAIN
GET RECEIVED SIGNAL STRENGTH
CLEAR REGISTER
POSITION 1ST DIGIT
CONVERT TO ASCII
STORE IN OUTPUT BUFFER
CLEAR REGISTER
POSITION LAST 2 DIGITS

CONVERT TO ASCII
STORE IN OUTPUT BUFFER
GET ADDRESS OF BUFFER TO OUTPUT
OUTPUT BUFFER
DONE
SPACE FOR PATCHES

TIME: 16:43:42 03/18/77

ATAC	LOC	OBJECT CODE	CARD	IMAGE	CARDNUM
0658	9C01 09F0	STR	D, WJVI, WJSCNT	INITIALIZE PASS COUNT	320
065A	E101 0B97	LDR	I, WJVI, WJSCAN	GET ADDRESS OF SCAN TITLE	321
065C	ED00 0230	BAL	I, RET, OUTPUT	OUTPUT SCAN TITLE	322
065E		DS	16	SPACE FOR PATCHES	323
					324
					325
					326
0668	E101 0B9C	IDR	I, WJVI, WJSFS	GET ADDRESS OF START FREQUENCY TITLE	327
066A	ED00 07AE	BAL	I, RET, WJ90	OUTPUT TITLE AND GET ENTRY	328
066C	C107 0668	BRCL	U, WJ601	ILLEGAL ENTRY	329
066E	ED00 07CC	EAL	I, RET, WJ91	MAKE SURE FREQ IS IN LEGAL BOUNDS	330
0670	C107 0668	BRCL	U, WJ601	ILLEGAL ENTRY	331
0672	9C03 09ED	STR	D, WJVI, WJSFLL	SAVE LOWER LIMIT (LOWER)	332
0674	9C04 09EC	STR	D, WJV4, WJSFLL	SAVE LOWER LIMIT (UPPER)	333
0676		DS	16	SPACE FOR PATCHES	334
					335
					336
					337
					338
0680	E101 0BA7	LDR	I, WJVI, WJSFE	GET ADDRESS OF END FREQ TITLE	339
0682	ED00 07AE	BAL	I, RET, WJ90	OUTPUT TITLE AND GET ENTRY	340
0684	C107 0680	BRCL	U, WJ602	ILLEGAL ENTRY	341
0686	ED00 07CC	EAL	I, RET, WJ91	MAKE SURE FREQ IS IN LEGAL BOUNDS	342
0688	C107 0680	BRCL	U, WJ602	ILLEGAL ENTRY	343
068A	9C03 09EB	STR	D, WJV3, WJSFLL	SAVE UPPER LIMIT (LOWER)	344
068C	9C04 09EA	STR	D, WJV4, WJSFLL	SAVE UPPER LIMIT (UPPER)	345
068E		DS	16	SPACE FOR PATCHES	346
					347
					348
					349
0698	E205 09EC	LDR	D, WJV5, WJSFLL	GET LOWER LIMIT (UPPER)	350
069A	B054	CHP	R, WJV4, WJV5	COMPARE UPPER AND LOWER LIMITS' (UPPER)	351
069B	C104 0668	BRCL	LT, WJ601	UPPER LIMIT LESS THAN LOWER	352
069D	C101 06AE	BRCL	GT, WJ603	NO NEED TO CHECK FURTHER	353
069F	E205 09ED	LDR	D, WJV5, WJSFLL	GET LOWER LIMIT (LOWER)	354
06A1	B053	CHP	R, WJV3, WJV5	COMPARE UPPER AND LOWER LIMITS (LOWER)	355
06A2	C106 0668	BRCL	LE, WJ601	LESS OR EQUAL, TRY AGAIN	356
06A4		DS	16	SPACE FOR PATCHES	357
					358
					359
					360
06AE	E101 0BB1	LDR	I, WJVI, WJSFI	GET ADDRESS OF FREQ INC TITLE	361
06E0	ED00 07AE	BAL	I, RET, WJ90	OUTPUT TITLE AND GET ENTRY	362
06E2	C107 06AE	BRCL	U, WJ603	ILLEGAL ENTRY	363
06E4	B033	SHD	RS, WJV3, 4	POSITION INCREMENT	364
06E5	2042	CHP	IS, WJV2, 4	COMPARE COUNT WITH MAX	365
06E6	C101 06AE	BRCL	GT, WJ603	ILLEGAL - TOO LARGE	366
06E8	B103 0800	CHP	IF, WJV3, 0800	COMPARE WITH MAX INCREMENT	367
06EA	C101 06AE	BRCL	GT, WJ603	ILLEGAL - TOO LARGE	368
06BC	2013	CHP	IS, WJV3, 1	COMPARE WITH MIN INCREMENT	369
06BD	C104 06AE	BRCL	LT, WJ603	ILLEGAL - TOO SMALL	370
06DE	9C03 09EE	STR	D, WJV3, WJSFIN	SAVE INCREMENT	371
06FF		DS	16	SPACE FOR PATCHES	372
06C1					

LOC	OBJECT CODE	CARD IMAGE	OUTPUT TITLE AND GET SIGNAL STRENGTH	GET ADDRESS OF SIGNAL ENTRY OUTPUT TILE AND GET ENTRY ILLEGAL ENTRY COMPARE WITH MAX VALUE ILLEGAL - TOO LARGE COMPARE COUNT WITH MAX ILLEGAL - TOO LARGE PUT SIGNAL STRENGTH IN REG 2 CONVERT BCD TO HEX MULTIPLY BY 127 ROUND SET UP DIVISOR DIVIDE BY 100 CLEAR ALL BUT VALUE WANTED STORE DESIRED SIGNAL STRENGTH SPACE FOR PATCHES	TITLE	CARDNUM
06C5	E101 0BEE	WJ604	LDR I, WJ604	GET ADDRESS OF SIGNAL ENTRY	373	
06C6	ED00 07AE		BAL I, RET, WJ90	OUTPUT TILE AND GET ENTRY	374	
06C7	C107 06CB		U, WJ604	ILLEGAL ENTRY	375	
06D1	B103 0100		CMP I, WJ3, 0100	COMPARE WITH MAX VALUE	376	
06D3	C101 06CB		BRCL I, WJ604	ILLEGAL - TOO LARGE	377	
06D5	2032		CHP I, WJ604	COMPARE COUNT WITH MAX	378	
06D6	C101 06CB		BRCL I, WJ604	ILLEGAL - TOO LARGE	379	
06D8	E032 09BE		LDR R, WJ604	PUT SIGNAL STRENGTH IN REG 2	380	
06D9	ED00 09BE		BAL I, RET, WJBCDH	CONVERT BCD TO HEX	381	
06EB	C001 007F		MUL I, WJ1, 07F	MULTIPLY BY 127	382	
06ED	6321		ADD I, WJ1, 032	ROUND	383	
06DE	A443		LDR IS, WJ3, 064	SET UP DIVISOR	384	
06DF	FC31		DIV R, WJ1, WJ3	DIVIDE BY 100	385	
06E0	A102 007F		AND I, WJ2, 07F	CLEAR ALL BUT VALUE WANTED	386	
06E2	9C02 09EF		STR D, WJ2, WJSFSS	STORE DESIRED SIGNAL STRENGTH	387	
06E4			DS 10	SPACE FOR PATCHES	388	
					389	
					390	
					391	
					392	
					393	
06EE	E205 09ED	WJ605	LDR D, WJ5, WJSFLL	GET LOWER LIMIT (LOWER)	394	
06EF	E206 09EC		LDR D, WJ6, WJSFLU	GET LOWER LIMIT (UPPER)	395	
06F2	F835		SHD LL, WJ5, 4	POSITION FREQUENCY FOR WJ	396	
06F3	E203 09C9	WJ606	LDR D, WJ3, WJCW2	GET CONTROL WORD 2 (FREQ LOWER)	397	
06F5	E204 09C8		LDR D, WJ4, WJCW1	GET CONTROL WORD 1 (FREQ UPPER)	398	
06F7	A103 000F		AND I, WJ3, 0F	CLEAR OLD FREQ (LOWER)	399	
06F9	A104 0000		AND I, WJ4, 0	CLEAR OLD FREQ (UPPER)	400	
06FB	A453		IOR R, WJ3, WJ5	PUT IN NEW FREQ (LOWER)	401	
06FC	A464		IOR R, WJ4, WJ6	PUT IN NEW FREQ (UPPER)	402	
06FD	9C03 09C9		STR D, WJ3, WJCW2	SAVE NEW CONTROL WORD 2	403	
06FE	9C04 09C8		STR D, WJ4, WJCW1	SAVE NEW CONTROL WORD 1	404	
06FF	ED00 08AE		I, RET, WJS	SEND /RECEIVE NEW CONTROL WORD	405	
0701			DS 10	SPACE FOR PATCHES	406	
0703					407	
					408	
					409	
					410	
070D	E201 09CF		LDR D, WJ1, WJRS4	GET RECEIVED WORD 4	411	
070F	A101 007F		AND I, WJ1, 07F	CLEAR ALL BUT SIGNAL STRENGTH	412	
0711	E202 09EF		LDR D, WJ2, WJSFSS	GET SPECIFIED SIGNAL STRENGTH	413	
0713	B021 074E		CHP R, WJ1, WJ2	COMPARE RECEIVED WITH SPECIFIED	414	
0714	C103 074E		BRCL R, WJ609	FIND	415	
0716			DS 10	SPACE FOR PATCHES	416	
					417	
					418	
					419	
					420	
0720	E201 09C9		LDR D, WJ1, WJCW2	GET LAST FREQ (LOWER)	421	
0722	E202 09C8		LDR D, WJ2, WJCW1	GET LAST FREQ (UPPER)	422	
0724	F831 03FF		SHD RL, WJ1, 4	POSITION FOR INCREMENT	423	
0725	A102 03FF		AND I, WJ2, 03FF	CLEAR ALL BUT FREQUENCY	424	
0727	E203 09EE		LDR D, WJ3, WJSFIN	GET INCREMENT	425	
0729	4004		IS, WJ4, 0	CLEAR REGISTER	426	
072A	ED00 0861		I, RET, WJ96	INCREMENT FREQUENCY	427	

03/18/77

TIME: 16:43:42

ATAC

LOC	OBJECT CODE	CARD IMAGE	CARDNUM
072C	E201 09EB	LDR D,WJVI,WJSF00	426
072E	E202 09EA	LDR D,WJVI,WJSF00	427
0730	E062	CMP R,WJVI,WJVI	428
0731	C101 06F2	BRCL R,WJVI,WJVI	429
0733	C102 073F	BRCL R,WJVI,WJVI	430
0735	E201 09F0	LDR D,WJVI,WJVI	431
0737	E011	ADD IS,WJVI,100	432
0738	2641	CMP IS,WJVI,100	433
0739	C101 075E	BRCL R,WJVI,WJVI	434
073B	9C01 09F0	STR D,WJVI,WJVI	435
073D	C107 06EE	BRCL R,WJVI,WJVI	436
073F	E051	CMP R,WJVI,WJVI	437
0740	C104 0735	BRCL R,WJVI,WJVI	438
0742	C107 06F2	BRCL R,WJVI,WJVI	439
0744		DS 10	440
		. FIND	441
		. WJ609	442
C74E	BC11 09E0	LDRM D,WJVI,WJVI,2	443
0750	9C11 09D8	STRM D,WJVI,WJVI,2	444
0752	C107 05DE	BRCL D,WJVI,WJVI,2	445
0754		DS 10	446
		. NO FIND - TELL OPERATOR	447
		. WJ610	448
075E	BC11 09E0	LDRM D,WJVI,WJVI,2	449
0760	9C11 09D8	STRM D,WJVI,WJVI,2	450
0762	E101 0ECA	LDR I,WJVI,WJVI,0	451
0764	E000 0230	FAL I,RET,OUTPUT	452
0766	C107 0519	BRCL U,WJ02	453
0768		DS 40	454
		. *****	455
		. RECEIVE CONTROL WORD FROM RECEIVER (COMMAND=6)	456
		. *****	457
		. WJ70	458
0790	E101 0001	LDR I,WJVI,01	459
0792	9C01 09F4	STR D,WJVI,CHKFLG1	460
0794	E000 08E1	DAL I,RET,CHK	461
0796	E101 0000	LDR I,WJVI,0	462
0798	9C01 09F4	STR D,WJVI,CHKFLG1	463
079A	C107 05DE	BRCL U,WJ40	464
079C	C107 0519	BRCL U,WJ02	465
079E		DS 10	466
		. *****	467
		. DONE (COMMAND=7)	468
		. *****	469
		. *****	470
		. *****	471
		. *****	472
		. *****	473
		. *****	474
		. *****	475
		. *****	476
		. *****	477
		. *****	478

ATAC
LOC
OBJECT CODE
CARD IMAGE

CARDNUM

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. *****
. WJ80      LLC      D,WJV1,WJCRF      LOAD "ADDRESS OFF"
.          ROUT      02,WJV1          TURN OFF INTERFACE
.          LDR       R,RET,WJRET      LOAD RETURN ADDRESS
.          BRC       R,RET           RETURN TO CALLER
.
.
. *****
. ROUTINE TO OUTPUT BUFFER AND GET ENTRY FROM KEYBOARD
. ENTRY: WJV1 ADDRESS OF BUFFER TO BE OUTPUT
. EXIT:  WJV2 NUMBER OF CHARACTERS ENTERED
.        WJV3 ENTRY {LOWER} BCD
.        WJV4 ENTRY {UPPER} BCD
. RETURN FOR ILLEGAL ENTRY
. RETURN+2 FOR ILLEGAL ENTRY
. *****
. WJ90      STR      D,RET,WJ90R      SAVE THE RETURN ADDRESS
.          BAL      I,RET,OUTPUT     OUTPUT BUFFER
.          LDR      I,RET,KEYMR      GET INPUT FROM KEYBOARD
.          LDR      IS,WJV3,0        CLEAR REGISTER
.          LDR      IS,WJV4,0        CLEAR REGISTER
.          LDR      IS,WJV5,0        CLEAR REGISTER
.          LDR      RX,WJV2,WJV5,WJV1 GET COUNT FROM KEYMR
.          LDR      R,WJV7,WJV2      SET UP INDEX FOR LOOP
.          LDR      D,RET,WJ90R      GET RETURN ADDRESS
.          ADD      IS,WJV7,-1        DECREMENT COUNT
.          BRC      R,4,RET          ILLEGAL IF NEG NOTHING ENTERED
.          ADD      IS,WJV1,1         INCREMENT BUFFER POINTER
.          LDR      RX,WJV6,WJV5,WJV1 GET ONE CHARACTER
.          LDR      IS,WJV6,030       COMPARE CHAR WITH ASCII ZERO
.          BRC      R,4,RET          ILLEGAL CHARACTER IS LESS
.          LDR      IS,WJV6,039       COMPARE WITH ASCII 9
.          BRC      R,1,RET          ILLEGAL CHARACTER IS GREATER
.          AND      I,WJV6,OF        CLEAR UPPER 12 BITS
.          SHD      LL,WJV3,4        POSITION ENTRY FOR NEW CHARACTER
.          LDR      R,WJV3,WJV6      OR IN NEW CHARACTER
.          ADD      IS,WJV7,-1        DECREMENT COUNT
.          NN,WJ90,1                KEEP GOING IF MORE CHARACTERS
.          BRC      IS,RET,2         INCREMENT RETURN ADDRESS
.          BRC      R,RET           LEGAL RETURN
.
.
. *****
. ROUTINE TO CHECK A FREQUENCY ENTRY AND MAKE SURE IT IS IN WJ
. FREQUENCY LIMITS
. ENTRY: WJV2 NUMBER OF CHARACTERS ENTERED
.        WJV3 FREQUENCY (LOWER) BCD,1 HZ RESOLUTION

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03/18/77

TIME: 16:43:42

ATAC

LOC	OBJECT CODE	CARD IMAGE	CARDNUM
0833	4002	LDR IS,WJV2,0	638
0834	F831	SHD LL,WJV1,4	639
0835	AE32	SHS LL,WJV2,4	640
0836	F831	SHD LL,WJV1,4	641
0837	A502	IOR I,WJV2,63030	642
0839	9C02	STR D,WJV2,WJDBF1	643
083B	4002	LDR JS,WJV2,0	644
083C	F831	SHD LL,WJV1,4	645
083D	AE32	SHS LL,WJV2,4	646
083E	F831	SHD LL,WJV1,4	647
083F	A502	IOR I,WJV2,63030	648
0841	9C02	STR D,WJV2,WJDBF1+1	649
0843	0AF6	LDR I,WJV1,WJDBF	650
0845	E101	BAI I,RET,OUTPUT	651
0847	E200	LDR D,RET,WJ90R	652
0849	BF07	BRC R,RET	653
			654
			655
			656
			657
			658
			659
			660
			661
			662
084A	9C00	STR D,RET,WJ90R	663
084C	4002	LDR IS,WJV2,0	664
084D	F871	SHD LL,WJV1,8	665
084E	A502	IOR I,WJV2,62030	666
0850	2030	STR D,WJV2,WJDRF1	667
0852	4002	LDR IS,WJV2,0	668
0853	F831	SHD LL,WJV1,4	669
0854	AE32	SHS LL,WJV2,4	670
0855	F831	SHD LL,WJV1,4	671
0856	A502	IOR I,WJV2,63030	672
0858	9C02	STR D,WJV2,WJDRF1+1	673
085A	0B14	LDR I,WJV1,WJDRF	674
085C	E101	BAI I,RET,OUTPUT	675
085E	E200	LDR D,RET,WJ90R	676
0860	BF07	BRC R,RET	677
			678
			679
			680
			681
			682
			683
			684
			685
			686
			687
			688
			689
			690

03/18/77

TIME: 16:43:42

ATAC

IOC	OBJECT CODE	CARD IMAGE	SAVE RETURN ADDRESS SET UP MASK CLEAR REGISTER DO 1ST DIGIT DO 2ND DIGIT DO 3RD DIGIT DO 4TH DIGIT DO 5TH DIGIT DO 6TH DIGIT DO 7TH DIGIT	PAGE
C861	9C00	09F1	STR	691
0863	E109	000F	LDR	692
0865	4005		LDR	693
0866	4006		LDR	694
0867	E017		LDR	695
0868	E038	08A4	EAL	696
0869	E000		LDR	697
086A	E075		LDR	698
086C	E017		LDR	699
086D	AD37		SHS	700
086E	E087		ADD	701
086F	E038		LDR	702
0870	AD38		LDR	703
0871	ED00	08A4	SHS	704
0873	AE37		BAL	705
0874	AE37		SHS	706
0875	A475		LDR	707
0876	E017		LDR	708
0877	AD77		SHS	709
0878	E087		ADD	710
0879	E038		LDR	711
087A	AD78		SHS	712
087C	ED00	08A4	BAL	713
087D	AE77		SHS	714
087E	A475		LDR	715
087F	E017		LDR	716
0880	AE77		SHS	717
0881	E087		ADD	718
0882	E038		LDR	719
0883	AD88		SHS	720
0885	ED00	08A4	BAL	721
0886	AE87		SHS	722
0887	A475		LDR	723
0888	E027		LDR	724
0889	E087		ADD	725
088A	E048	08A4	LDR	726
088C	ED00		EAL	727
088D	E076		LDR	728
088E	E027		LDR	729
088F	AD37		SHS	730
0890	E087		ADD	731
0891	E048		LDR	732
0892	ED00	08A4	SHS	733
0894	AE37		BAL	734
0895	A476		SHS	735
0896	E027		LDR	736
0897	AD77		SHS	737
0898	E087		ADD	738
0899	E048		LDR	739
089A	AD78		SHS	740
089B	ED00	08A4	BAL	741
089D	AE77		SHS	742
				743

CARDNUM

ATAC

CARD IMAGE

OBJECT CODE

LOC

0925	E831	SHD	RL, WJV1, 4	POSITION FREQUENCY FOR DISPLAY	850
0926	A102	AND	I, WJV2, 03FF	CLEAR ALL BUT FREQUENCY	851
0928	9C01	STR	D, WJV1, WJREFL	STORE IN RECEIVED DISPLAY {LOWER}	852
092A	9C02	STR	D, WJV2, WJREFU	STORE IN RECEIVED DISPLAY {UPPER}	853
092C	E201	LDR	I, WJV1, 09CD	GET RECEIVED WORD 2	854
092E	A101	AND	I, WJV1, 0C	CLEAR ALL BUT GAIN MODE	855
0930	AD11	SHS	RL, WJV1, 2	POSITION GAIN MODE	856
0931	9C01	STR	D, WJV1, WJRGH	STORE IN RECEIVED GAIN MODE FOR DISP	857
0933	E201	LDR	D, WJV1, WJRS3	GET RECEIVED WORD 3	858
0935	E202	LDR	D, WJV2, WJRS2	GET RECEIVED WORD 2	859
0937	F801	SHD	LL, WJV1, 1	POSITION RECEIVED BANDWIDTH	860
0938	A102	AND	I, WJV2, 07	CLEAR ALL BUT BANDWIDTH	861
093A	9C02	STR	D, WJV2, WJRF	STORE IN RECEIVED DISPLAY	862
093C	A101	AND	I, WJV1, 0E00	CLEAR ALL BUT DETECT MODE	863
093E	ADC1	SHS	RL, WJV1, 13	POSITION DETECT MODE	864
093F	9C01	STR	D, WJV1, WJRDH	STORE IN RECEIVED DISPLAY	865
0941	E101	LDR	I, WJV1, 04	GET BFO UPPER DISPLAY	866
0943	9C01	STR	D, WJV1, WJRBH	STORE IN RECEIVED DISPLAY	867
0945	E201	LDR	D, WJV1, WJRS3	GET RECEIVED BFO FREQUENCY	868
0947	A101	AND	I, WJV1, 07FF	CLEAR ALL BUT BFO FREQUENCY	869
0949	4002	LDR	IS, WJV2, 0	CLEAR REG 2	870
094A	CD01	MUL	I, WJV1, 07D0	MULTIPLY BY 2000	871
094C	E103	LDR	I, WJV3, 07FF	LOAD DIVISOR	872
094E	E101	ADD	I, WJV1, 0400	ROUND	873
0950	FC31	DIV	R, WJV1, WJV3	DIVIDE	874
0951	AD12	ADD	I, WJV2, 01194	ADD 4500	875
0953	4003	LDR	IS, WJV3, 0	CLEAR REG 3	876
0954	40A4	LDR	IS, WJV4, 10	SET UP DIVISOR	877
0955	EC42	DIV	R, WJV2, WJV4	DIVIDE BY 10	878
0956	E021	LDR	R, WJV1, WJV2	PUT REMAINDER IN WJV1 AS 1ST DIGIT	879
0957	E032	LDR	R, WJV2, WJV3	GET QUOTIENT	880
0958	4003	LDR	IS, WJV3, 0	CLEAR REGISTER	881
0959	FC42	DIV	R, WJV2, WJV4	DIVIDE BY 10	882
095A	AE32	SHS	LL, WJV2, 4	POSITION 2ND DIGIT	883
095B	A421	IOR	R, WJV1, WJV2	PUT 2ND DIGIT IN ANSWER	884
095C	E032	LDR	R, WJV2, WJV3	GET QUOTIENT	885
095D	4003	LDR	IS, WJV3, 0	CLEAR REGISTER	886
095E	FC42	DIV	LL, WJV2, WJV4	DIVIDE BY 10	887
095F	AE72	SHS	LL, WJV2, 8	POSITION 3RD DIGIT	888
0960	AE33	SHS	LL, WJV3, 12	POSITION 4TH DIGIT	889
0961	A421	IOR	R, WJV1, WJV2	PUT IN 3RD DIGIT	890
0962	A431	IOR	R, WJV1, WJV3	PUT IN 4TH DIGIT	891
0963	9C01	STR	D, WJV1, WJREL	STORE IN RECEIVED BFO FREQ DISPLAY (892
0965	E202	LDR	D, WJV2, WJRS4	GET RECEIVED WORD 4	893
0967	A102	AND	I, WJV2, 07F00	CLEAR ALL BUT RF GAIN	894
0969	AD72	SHS	RL, WJV2, 8	RIGHT JUSTIFY	895
096A	B421	LLC	R, WJV1, WJV2	COMPLEMENT	896
096B	A101	AND	I, WJV1, 07F	CLEAR ALL BUT RF GAIN	897
096D	E000	EAL	I, RET, WJRS3	CONVERT TO BCD PERCENTAGE	898
096F	9C01	STR	D, WJV1, WJRRFG	STORE IN RECEIVED DISPLAY	899
0971	E201	LDR	D, WJV1, WJRS4	GET RECEIVED WORD 4	900
0973	A101	AND	I, WJV1, 07F	CLEAR ALL BUT SIGNAL STRENGTH	901
0975	E000	BAL	I, RET, WJRS3	CONVERT TO BCD PERCENTAGE	902

LOC	OBJECT CODE	CARD IMAGE	STORE IN RECEIVED DISPLAY	CARDNUM
0977	9C01 09E9	STR	GET RETURN ADDRESS	903
0979	E200 09F1	LDR	RETURN TO CALLER	904
097B	BF07	ERC		905
				906
097C	CD01 0064	MUL	MULTIPLY BY 100	907
097E	6371	ADD	ROUND	908
097F	47F3	ADD	SET UP DIVISOR	909
0980	FC31	DIV	DIVIDE BY 127	910
0981	E021	DIV	PUT DIVIDEND IN REG 1	911
0982	4002	LDR	CLEAR REGISTER	912
0983	40A3	LDR	SET UP DIVISOR	913
0984	FC31	DIV	DIVIDE BY 10	915
0985	E014	LDR	PUT REMAINDER IN REG 4 (DIGIT 1)	916
0986	E021	LDR	SET UP DIVIDEND	917
0987	4002	LDR	CLEAR REGISTER	918
0988	FC31	DIV	DIVIDE BY 10	919
0989	AE31	SMS	POSITION 3RD DIGIT	920
098A	AE72	SMS	POSITION 2ND DIGIT	921
098B	A441	IOR	COMBINE 1ST AND 2ND DIGITS	922
098C	A421	IOR	COMBINE ALL DIGITS	923
098D	BF07	ERC	RETURN TO CALLER	924
				925
				926
				927
				928
				929
				930
				931
				932
				933
				934
098E	E021	LDR	LOAD LEAST SIGNIFICANT BITS, PART 1	935
098F	A101 000F	AND	" "	936
0991	AD32	SMS	SHIFT FOR MULTIPLICATION	937
0992	E023	LDR	LOAD DUMMY REG FOR MULTIPLICATION	938
0993	A103 000F	AND	CLEAR ALL BUT LEAST SIG BITS	939
0995	CD03 000A	MUL	MULTIPLY BY 16	940
0997	8031	ADD	ADD CRYPTO ANSWER	941
0998	AD32	SMS	SHIFT FOR MULTIPLICATION	942
0999	E023	LDR	LOAD DUMMY REG FOR MULTIPLICATION	943
099A	A103 000F	AND	CLEAR ALL BUT LEAST SIG BITS	944
099C	CD03 0064	MUL	MULTIPLY BY 100	945
099E	8031	ADD	ADD CRYPTO ANSWER	946
099F	AD32	SMS	SHIFT FOR MULTIPLICATION	947
09A0	CD02 03E8	MUL	MULTIPLY BY 1000	948
09A2	8021	ADD	ADD CRYPTO ANSWER	949
09A3	BF07	ERC	RETURN TO CALLER	950
				951
				952
				953
				954

03/18/77

TIME: 16:43:42

ATAC

LOC	OBJECT CODE	CARD IMAGE	RCVR CONTROL WORD	CARDNUM
09C8		WJCH1 DS 1	1	1008
09C9		WJCH2 DS 1	2	1009
09CA		WJCH3 DS 1	3	1010
09CB		WJCH4 DS 1	4	1011
09CC		RECEIVED WORD FROM WJ		1012
09CD		WJRS1 LS 1	1	1013
09CE		WJRS2 DS 1	2	1014
09CF		WJRS3 DS 1	3	1015
		WJRS4 DS 1	4	1016
09D0		TENTATIVE VALUES - DISPLAY FORMAT		1017
09D1		WJFLL DS 1		1018
09D2		WJTFU DS 1		1019
09D3		WJTFM DS 1		1020
09D4		WJTBLL DS 1		1021
09D5		WJTBH DS 1		1022
09D6		WJTCM DS 1		1023
09D7		WJTRFG DS 1		1024
		WJTRIF DS 1		1025
09D8		CONTROL VALUES - DISPLAY FORMAT		1026
09D9		WJCP1 DS 1		1027
09DA		WJCFU DS 1		1028
09DB		WJCDM DS 1		1029
09DC		WJCBLL DS 1		1030
09DD		WJCGM DS 1		1031
09DE		WJCRFG DS 1		1032
09DF		WJCIF DS 1		1033
09E0		RECEIVED VALUES - DISPLAY FORMAT		1034
09E1		WJRFLL DS 1		1035
09E2		WJRFU DS 1		1036
09E3		WJRDM DS 1		1037
09E4		WJRBL DS 1		1038
09E5		WJRBH DS 1		1039
09E6		WJRCM DS 1		1040
09E7		WJTRFG DS 1		1041
09E8		WJTRIF DS 2		1042
09E9		WJRSS DS 1		1043
09EA		SCAN VARIABLES		1044
09EB		WJSEU DS 1		1045
09EC		WJSFUL DS 1		1046
09ED		WJSFLU DS 1		1047
09EE		WJSFLI DS 1		1048
09EF		WJSFIN DS 1		1049
09F0		WJSFSS DS 1		1050
		WJSCNT DS 1		1051
		SAVE LOCATIONS FOR ALL WJ9- ROUTINES		1052
		RECEIVED FREQUENCY {LOWER}		1053
		RECEIVED DETECT MODE		1054
		RECEIVED BFO FREQUENCY {LOWER}		1055
		RECEIVED BFO FREQUENCY {UPPER}		1056
		RECEIVED GAIN MCDE		1057
		RECEIVED RF GAIN		1058
		RECEIVED IF BANDWIDTH		1059
		RECEIVED SIGNAL STRENGTH		1060
		UPPER LIMIT {UPPER}		
		UPPER LIMIT {LOWER}		
		LOWER LIMIT {UPPER}		
		LOWER LIMIT {LOWER}		
		FREQUENCY INCREMENT (8 KHZ MAX)		
		SIGNAL STRENGTH		
		COUNT OF NUMBER OF SCAN PASSES		

CARDNUM

CARD IMAGE

OBJECT CODE

LOC

LOC	OBJECT CODE	CARD IMAGE	CARDNUM
0A21	5245	DC	1114
0A22	4345	DC	1115
0A23	4956	DC	1116
0A24	4544	DC	1117
0A25	0D0A	DC	1118
0A26	343D	EC	1119
0A27	454E	EC	1120
0A28	5445	DC	1121
0A29	5220	DC	1122
0A2A	5445	EC	1123
0A2B	4E54	EC	1124
0A2C	4154	DC	1125
0A2D	4956	EC	1126
0A2E	450D	EC	1127
0A2F	0A35	EC	1128
0A30	3D53	EC	1129
0A31	4341	EC	1130
0A32	4E20	EC	1131
0A33	0D0A	DC	1132
0A34	363D	DC	1133
0A35	5245	EC	1134
0A36	4345	DC	1135
0A37	4956	EC	1136
0A38	4520	DC	1137
0A39	434F	DC	1138
0A3A	4E54	DC	1139
0A3B	524F	DC	1140
0A3C	4C20	DC	1141
0A3D	0D0A	EC	1142
0A3E	373D	DC	1143
0A3F	444F	DC	1144
0A40	4E45	DC	1145
0A41	0D0A	EC	1146
0A42	383D	EC	1147
0A43	5245	DC	1148
0A44	494E	DC	1149
0A45	4954	DC	1150
0A46	494C	DC	1151
0A47	495A	DC	1152
0A48	4520	DC	1153
0A49	0D0A	EC	1154
0A4A	0000	DC	1155
0A4B	0006	DC	1156
0A4C	4652	DC	1157
0A4D	4551	DC	1158
0A4E	2028	DC	1159
0A4F	485A	DC	1160
0A50	2920	DC	1161
0A51	0D0A	DC	1162
0A52	0000	DC	1163
		CR/LF	1164
		NULL	1165
		NULL	1166

WJFB : FREQUENCY TITLE BUFFER

COUNT
FR
EQ
H2
CR/LF
NULL

ATAC

LOC	OBJECT CODE	CARD IMAGE	COUNT	CARDNUM
0AE5	0007	DC	DE	1326
0AE6	4445	DC	TE	1327
0AE7	5445	DC	CT	1328
0AE8	4354	DC	M	1329
0AE9	204D	DC	OD	1330
0AEA	4F44	DC	E	1331
0AEB	4520	DC	=	1332
0AEC	3D20	DC	NULL	1333
0AED	0000	DC		1334
				1335
				1336
0AEE	000B	DC	BF	1337
0AEF	4246	DC	O	1338
0AF0	4F20	DC	FR	1339
0AF1	4652	DC	EQ	1340
0AF2	4551	DC	=	1341
0AF3	203D	DC	4	1342
0AF4	2034	DC	XX	1343
0AF5	2020	DC	XX	1344
0AF6	2020	DC	O	1345
0AF7	3020	DC	RZ	1346
0AF8	485A	DC	CR/LF	1347
0AF9	000A	DC	NULL	1348
0AFA	0000	DC		1349
				1350
0AFB	0006	DC	GA	1351
0AFC	4741	DC	IN	1352
0AFD	494E	DC	M	1353
0AEE	204D	DC	OD	1354
0AEF	4F44	DC	E	1355
0B00	4520	DC	=	1356
0B01	3D20	DC	NULL	1357
0B02	0000	DC		1358
				1359
0B03	0008	DC	IF	1360
0B04	4946	DC	B	1361
0B05	2042	DC	AN	1362
0B06	414E	DC	AW	1363
0B07	4457	DC	DW	1364
0B08	4944	DC	ID	1365
0B09	5448	DC	TH	1366
0B0A	203D	DC	=	1367
0B0B	2020	DC	NULL	1368
0B0C	0000	DC		1369
				1370
0B0D	0009	DC	RF	1371
0B0E	5246	DC	G	1372
0B0F	2047	DC	AI	1373
0B10	4149	DC	N	1374
0B11	4E20	DC		1375
				1376
				1377

ATAC	IOC	OBJECT CODE	CARD IMAGE	CARDNUM
OB12	3D20		DC 03D20	1379
OB13	2020	WJDRF1	DC XX	1380
OB14	2020		DC XX	1381
OB15	2520		DC XX	1382
OB16	0D0A		DC CR/LF	1383
OB17	0000		DC NULL	1384
. SIGNAL STRENGTH TITLE FOR DISPLAY				
OB18	000D	WJDSS	DC 13	1385
OB19	5349		DC SI	1386
OB1A	474E		DC GN	1387
OB1B	414C		DC AL	1388
OB1C	2053		DC S	1389
OB1D	5452		DC TR	1390
OB1E	454E		DC EN	1391
OB1F	4754		DC GT	1392
OB20	4820		DC H	1393
OB21	3D20		DC =	1394
OB22	2020	WJDSS1	DC XX	1395
OB23	2020		DC XX	1396
OB24	2520		DC %	1397
OB25	0D0A		DC CR/LF	1398
OB26	0000		DC NULL	1399
. TABLE OF GAIN MODES FOR DISPLAY				
OB27	0B2B	WJGM1B	DC WJGM0	1400
OB28	0B32		DC WJGM1	1401
OB29	0B34		DC WJGM2	1402
OB2A	0B3C		DC WJGM3	1403
. WJGM0				
OB2B	0005		DC 5	1404
OB2C	484F		DC 0484F	1405
OB2D	4C44		DC 04C44	1406
OB2E	2041		DC 02041	1407
OB2F	4743		DC 04743	1408
OB30	0D0A		DC 00D0A	1409
OB31	0000		DC 0	1410
. WJGM1				
OB32	FFFF		DC -1	1411
OB33	0000		DC 0	1412
. WJGM2				
OB34	0006		DC 6	1413
OB35	4E4F		DC 04E4F	1414
OB36	524D		DC 0524D	1415
OB37	414C		DC 0414C	1416
OB38	2041		DC 02041	1417
OB39	4743		DC 04743	1418
OB3A	0D0A		DC 00D0A	1419
OB3B	0000		DC 0	1420
. COUNT/NORMAL AGC				
OB34	0006		DC NO	1421
OB35	4E4F		DC RM	1422
OB36	524D		DC AL	1423
OB37	414C		DC A	1424
OB38	2041		DC GC	1425
OB39	4743		DC CR/LF	1426
OB3A	0D0A		DC NULL	1427
OB3B	0000		DC	1428
. COUNT/HOLD AGC				
OB34	0006		DC HO	1429
OB35	4E4F		DC LD	1430
OB36	524D		DC A	1431
OB37	414C		DC GC	1432
OB38	2041		DC CR/LF	1433
OB39	4743		DC NULL	1434
OB3A	0D0A		DC	1435
OB3B	0000		DC	1436

LOC	OBJECT CODE	CARD IMAGE	CARDNUM
0B3C	0004	DC	1432
0B3D	4D41	DC	1433
0B3E	4E55	EC	1434
0B3F	414C	EC	1435
0B40	0D0A	DC	1436
0B41	0000	DC	1437
			1438
			1439
			1440
0B42	0B47	DC	1441
0B43	0B49	DC	1442
0B44	0B4F	DC	1443
0B45	0B55	DC	1444
0B46	0B5B	DC	1445
			1446
			1447
0B47	FFFF	DC	1448
0B48	0000	EC	1449
			1450
0B49	0004	DC	1451
0B4A	3530	EC	1452
0B4B	3020	DC	1453
0B4C	4B5A	DC	1454
0B4D	000A	DC	1455
0B4E	0000	DC	1456
			1457
			1458
			1459
0B4F	0004	DC	1460
0B50	3220	DC	1461
0B51	4B48	DC	1462
0B52	5A20	LC	1463
0B53	0D0A	DC	1464
0B54	0000	DC	1465
			1466
			1467
0B55	0004	DC	1468
0B56	3420	DC	1469
0B57	4B48	DC	1470
0B58	5A20	DC	1471
0B59	0D0A	DC	1472
0B5A	0000	DC	1473
			1474
			1475
0B5B	0004	DC	1476
0B5C	3820	DC	1477
0B5D	4B48	DC	1478
0B5E	5A20	LC	1479
0B5F	0D0A	DC	1480
0B60	0000	DC	1481
			1482
			1483
0B61	0B69	DC	1484

TABLE CF IF BANDWIDTHS FOR DISPLAY

WJIFB DC WJIF0 NOT USED

WJIF1 500HZ

WJIF2 2KHZ

WJIF3 4KHZ

WJIF4 8KHZ

WJIF0 -1 COUNT/INVALID ENTRY

WJIF1 4 COUNT/500KHZ

WJIF2 0 50

WJIF3 0 HZ

WJIF4 0 CR/LF

WJIF5 0 NULL

WJIF6 2 COUNT/2KHZ

WJIF7 0 KH

WJIF8 0 Z

WJIF9 0 CR/LD

WJIFA 0 NULL

WJIFB 4 COUNT/4KHZ

WJIFC 0 KH

WJIFD 0 Z

WJIFE 0 CR/LF

WJIFF 0 NULL

WJIFG 4 COUNT/8 KHZ

WJIFH 0 KH

WJIFI 0 Z

WJIFJ 0 CR/LF

WJIFK 0 NULL

WJIFL 4 COUNT/8 KHZ

WJIFM 0 KH

WJIFN 0 Z

WJIFO 0 CR/LF

WJIFP 0 NULL

WJIFQ 4 COUNT/8 KHZ

WJIFR 0 KH

WJIFS 0 Z

WJIFT 0 CR/LF

WJIFU 0 NULL

WJIFV 4 COUNT/8 KHZ

WJIFW 0 KH

WJIFX 0 Z

WJIFY 0 CR/LF

WJIFZ 0 NULL

WJIFA 4 COUNT/8 KHZ

WJIFB 0 KH

WJIFC 0 Z

WJIFD 0 CR/LF

WJIFE 0 NULL

WJIFF 4 COUNT/8 KHZ

WJIFG 0 KH

WJIFH 0 Z

WJIFI 0 CR/LF

WJIFJ 0 NULL

WJIFK 4 COUNT/8 KHZ

WJIFL 0 KH

WJIFM 0 Z

WJIFN 0 CR/LF

WJIFO 0 NULL

WJIFP 4 COUNT/8 KHZ

WJIFQ 0 KH

WJIFR 0 Z

WJIFS 0 CR/LF

WJIFT 0 NULL

WJIFU 4 COUNT/8 KHZ

WJIFV 0 KH

WJIFW 0 Z

WJIFX 0 CR/LF

WJIFY 0 NULL

WJIFZ 4 COUNT/8 KHZ

WJIFA 0 KH

WJIFB 0 Z

WJIFC 0 CR/LF

WJIFD 0 NULL

WJIFE 4 COUNT/8 KHZ

WJIFF 0 KH

WJIFG 0 Z

WJIFH 0 CR/LF

WJIFI 0 NULL

WJIFJ 4 COUNT/8 KHZ

WJIFK 0 KH

WJIFL 0 Z

WJIFM 0 CR/LF

WJIFN 0 NULL

WJIFO 4 COUNT/8 KHZ

WJIFP 0 KH

WJIFQ 0 Z

WJIFR 0 CR/LF

WJIFS 0 NULL

WJIFT 4 COUNT/8 KHZ

WJIFU 0 KH

WJIFV 0 Z

WJIFW 0 CR/LF

WJIFX 0 NULL

WJIFY 4 COUNT/8 KHZ

WJIFZ 0 KH

WJIFA 0 Z

WJIFB 0 CR/LF

WJIFC 0 NULL

WJIFD 4 COUNT/8 KHZ

WJIFE 0 KH

WJIFF 0 Z

WJIFG 0 CR/LF

WJIFH 0 NULL

WJIFI 4 COUNT/8 KHZ

WJIFJ 0 KH

WJIFK 0 Z

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WJIFM 0 NULL

WJIFN 4 COUNT/8 KHZ

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WJIFR 0 NULL

WJIFS 4 COUNT/8 KHZ

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WJIFE 0 Z

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WJIFK 0 CR/LF

WJIFL 0 NULL

WJIFM 4 COUNT/8 KHZ

WJIFN 0 KH

WJIFO 0 Z

WJIFP 0 CR/LF

WJIFQ 0 NULL

WJIFR 4 COUNT/8 KHZ

WJIFS 0 KH

WJIFT 0 Z

WJIFU 0 CR/LF

WJIFV 0 NULL

WJIFW 4 COUNT/8 KHZ

WJIFX 0 KH

WJIFY 0 Z

WJIFZ 0 CR/LF

WJIFA 0 NULL

WJIFB 4 COUNT/8 KHZ

WJIFC 0 KH

WJIFD 0 Z

WJIFE 0 CR/LF

WJIFF 0 NULL

WJIFG 4 COUNT/8 KHZ

WJIFH 0 KH

WJIFI 0 Z

WJIFJ 0 CR/LF

WJIFK 0 NULL

WJIFL 4 COUNT/8 KHZ

WJIFM 0 KH

WJIFN 0 Z

WJIFO 0 CR/LF

WJIFP 0 NULL

WJIFQ 4 COUNT/8 KHZ

WJIFR 0 KH

WJIFS 0 Z

WJIFT 0 CR/LF

WJIFU 0 NULL

WJIFV 4 COUNT/8 KHZ

WJIFW 0 KH

WJIFX 0 Z

WJIFY 0 CR/LF

WJIFZ 0 NULL

WJIFA 4 COUNT/8 KHZ

WJIFB 0 KH

WJIFC 0 Z

WJIFD 0 CR/LF

WJIFE 0 NULL

WJIFF 4 COUNT/8 KHZ

WJIFG 0 KH

WJIFH 0 Z

WJIFI 0 CR/LF

WJIFJ 0 NULL

WJIFK 4 COUNT/8 KHZ

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WJIFP 0 KH

WJIFQ 0 Z

WJIFR 0 CR/LF

WJIFS 0 NULL

WJIFT 4 COUNT/8 KHZ

WJIFU 0 KH

WJIFV 0 Z

WJIFW 0 CR/LF

WJIFX 0 NULL

WJIFY 4 COUNT/8 KHZ

WJIFZ 0 KH

03/18/77

TIME: 16:43:42

ATAC

LOC	OBJECT CODE	CARD IMAGE	CARDNUM	PAGE
OB62	OB6D	DC	1485	
OB63	OB71	DC	1486	
OB64	OB79	DC	1487	
OB65	OB82	DC	1488	
OB66	OB87	DC	1489	
OB67	OB8C	DC	1490	
OB68	OB91	LC	1491	
			1492	
			1493	
OB69	0002	DC	1494	
OB6A	414D	DC	1495	
OB6B	0D0A	DC	1496	
OB6C	0000	DC	1497	
			1498	
			1499	
OB6D	0002	DC	1500	
OB6E	464D	DC	1501	
OB6F	0D0A	DC	1502	
OB70	0000	DC	1503	
			1504	
			1505	
OB71	0006	DC	1506	
OB72	4246	DC	1507	
OB73	4F20	DC	1508	
OB74	4649	DC	1509	
OB75	5845	DC	1510	
OB76	4420	LC	1511	
OB77	0D0A	DC	1512	
OB78	0000	LC	1513	
			1514	
			1515	
OB79	0007	DC	1516	
OB7A	4246	LC	1517	
OB7B	4F20	DC	1518	
OB7C	5641	DC	1519	
OB7D	5249	DC	1520	
OB7E	4142	DC	1521	
OB7F	4C45	LC	1522	
OB80	0D0A	DC	1523	
OB81	0000	DC	1524	
			1525	
			1526	
OB82	0003	DC	1527	
OB83	4953	DC	1528	
OB84	4220	DC	1529	
OB85	0D0A	DC	1530	
OB86	0000	DC	1531	
			1532	
			1533	
OB87	0003	DC	1534	
OB88	4C53	LC	1535	
OB89	4220	DC	1536	
OB8A	0D0A	DC	1537	

ATAC	LOC	OBJECT CODE	CARD IMAGE	CARDNUM
OB8B	0000		DC 0	1538 1539 1540 1541 1542 1543 1544 1545 1546 1547 1548 1549 1550 1551 1552 1553 1554 1555 1556 1557 1558 1559 1560 1561 1562 1563 1564 1565 1566 1567 1568 1569 1570 1571 1572 1573 1574 1575 1576 1577 1578 1579 1580 1581 1582 1583 1584 1585 1586 1587 1588 1589 1590
OB8C	0003		DC	NULL
OB8D	5553	WJDM7	DC	COUNT/USB
OB8E	4220		DC	US
OB8F	0D0A		DC	B
OB90	0000		DC	CR/LF
OB91	0004		DC	NULL
OB92	414D	WJDM8	DC	COUNT/AM-NL
OB93	2D4E		DC	AM
OB94	4C20		DC	-N
OB95	0D0A		DC	L
OB96	0000		DC	CR/LF
OB97	0003		DC	NULL
OB98	5343		DC	COUNT
OB99	414E	WJSCAN	DC	SC
OB9A	0D0A		DC	AM
OB9B	0000		DC	CR/LF
OB9C	0009		DC	NULL
OB9D	5354		DC	COUNT
OB9E	4152		DC	ST
OB9F	5420		DC	AR
OB9A	4652		DC	T
OB9A	4551		DC	FR
OB9A	2049		DC	EQ
OB9A	4E20		DC	I
OB9A	485A		DC	N
OB9A	0D0A		DC	HZ
OB9A	0000		DC	CR/LF
OB9A	0000		DC	NULL
OB9A	0008		DC	COUNT
OB9A	454E		DC	EN
OB9A	4420		DC	D
OB9A	4652		DC	FR
OB9A	4551		DC	EQ
OB9A	2049		DC	I
OB9A	4E20		DC	N
OB9A	485A		DC	HZ
OB9A	0D0A		DC	CR/LF
OB9A	0000		DC	NULL
OB9A	0008		DC	COUNT
OB9A	454E		DC	EN
OB9A	4420		DC	D
OB9A	4652		DC	FR
OB9A	4551		DC	EQ
OB9A	2049		DC	I
OB9A	4E20		DC	N
OB9A	485A		DC	HZ
OB9A	0D0A		DC	CR/LF
OB9A	0000		DC	NULL
OB9A	000B		DC	COUNT
OB9A	4652		DC	FR
OB9A	4551		DC	EQ

TIME: 16:43:42

03/18/77

PAGE

CARDNUM

1644
1645
1646
1647
1648
1649
1650
1651
1652
1653
1654
1655
1656
1657
1658
1659

IN
TE
RF
AC
E
AN
D
RE
CE
IV
ER
BE
CR/LF
NULL

0494E
05045
05246
04143
04520
0414E
04420
05245
04345
04956
04552
00707
00D0A
0000

CARD IMAGE

DC
DC
DC
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DC

PAGE

ATAC

LOC OBJECT CODE

0BE2 494E
0BE3 5445
0BE4 5246
0BE5 4143
0BE6 4520
0BE7 414E
0BE8 4420
0BE9 5245
0BEA 4345
0BEB 4956
0BEC 4552
0BED C707
0BEE 0D0A
0BEF 0000

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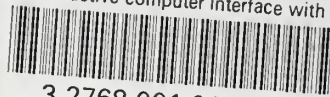
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